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13. ABSTRACT *(Maximum 200 words)*

By any measure of productivity and impact this program has been highly productive and has had a major impact on III-V semiconductor technology as evidenced by the number of publications, graduate-student output, interactions with Army laboratories, and other D.O.D., industrial and academic laboratories. This program has provided tremendous leverage by enabling us to attract major programs from other federal agencies and industry. It has also enabled us to establish one of the leading facilities and programs in the nation for research in high-frequency microelectronics through major cost-sharing by the University, the State of Michigan and industrial and federal agencies. This program has had and will continue to have a tremendous impact on the field.

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3. TITLE OF PROPOSAL: High-Frequency Microelectronics
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7. SUMMARY OF MAJOR ACCOMPLISHMENTS AND A LIST OF MANUSCRIPTS SUBMITTED OR PUBLISHED UNDER ARO SPONSORSHIP DURING THIS REPORTING PERIOD, INCLUDING JOURNAL REFERENCES.

By any measure of productivity and impact this program has been highly productive and has had a major impact on III-V semiconductor technology as evidenced by the number of publications, graduate-student output, interactions with Army laboratories, and other D.O.D., industrial and academic laboratories. This program has provided tremendous leverage by enabling us to attract major programs from other federal agencies and industry. It has also enabled us to establish one of the leading facilities and programs in the nation for research in high-frequency microelectronics through major cost-sharing by the University, the State of Michigan and industrial and federal agencies. This program has had and will continue to have a tremendous impact on the field. The following presents a summary of major accomplishments under this program:

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7.1 PUBLICATIONS

The manuscripts published or submitted under the Army Research Office sponsorship includes:

1. A publication summary
2. A detailed list of publications including journal references.

PUBLICATION SUMMARY

BOOK CHAPTERS			TOTAL
	1992	0	
	1993	0	
	1994	0	
	1995	0	
	1996	0	
	1997	0	
	1998	0	0
JOURNAL PUBLICATIONS			
	1992	15	
	1993	31	
	1994	43	
	1995	33	
	1996	36	
	1997	26	
	1998	9	193
CONFERENCE PRESENTATIONS			
	1992	15	
	1993	39	
	1994	16	
	1995	40	
	1996	23	
	1997	16	
	1998	11	160
	TOTAL		353
Accepted for Journal Publication (1998)			2
Accepted for Conference Presentation (1998)			0
Submitted to Journals			2
Submitted to Conferences			0
		(Total Pending	4)
GRAND TOTAL			357

PUBLICATION LIST

CENTER FOR HIGH-FREQUENCY MICROELECTRONICS

ACCEPTED PUBLICATIONS AND CONFERENCE PRESENTATIONS
(AND CURRENT SUBMISSIONS)

1. J. Singh, Y. Arakawa and P. K. Bhattacharya, "Consequences of Structural Disorder on Laser Properties in Quantum Wires Lasers," *Photonic Technology Letters*, **4**, 835 –837, 1992.

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112. S. Kulkarni, P. Mazumder and G. Haddad, "A High-Speed 32-bit Parallel Correlator for Spread Spectrum Communication," presented at the 9th International Conference on VLSI Design, Bangalore, India, January, 1996.

113. D. Sawdai, K. Hong and D. Pavlidis, "High Power Performance InP/InGaAs Single HBTs," presented at the 22nd International Symposium on Compound Semiconductors, Cheju Island, Korea, August, 1995; Inst. Phys. Conf. Ser. No. 145, Chapter 4, pp. 621-626, 1996.

114. K. C. Syao, A. L. Gutierrez-Aitken, K. Yang, X. Zhang, G. Haddad and P. Bhattacharya, "A Novel Technique to Reduce Crosstalk in Monolithically Integrated High Speed Photoreceiver Arrays," *Techn. Digest of IEDM'97*, San Francisco, California, pp. 649-652, December 8-11, 1996.

115. C. Y. Sung, X. Zhang, T. B. Norris and G. I. Haddad, "Time-Resolved Population Inversion in Intersubband FIR Laser Structures and Femtosecond Intersubband Relaxations," presented at SPIE International Conf. on Quantum Well and Superlattice Physics VI, San Jose, California, January 27-February 2, 1996.

116. X. Zhang, C. Y. Sung, T. B. Norris and G. Haddad, "Population Inversion in Asymmetrical Step Quantum Wells and Infrared Intersubband Lasers," *Proc. of SPIE*, **2694**, 19, 1996.

117. C. Y. Sung, T. B. Norris, Y. Lam, J. Singh, X. Zhang and P. Bhattacharya, "Gain Recovery Dynamics: Femtosecond Time-Resolved Spectral Hole Burning and Carrier Capture in Separate-Confinement QW Laser Structure," presented at the Conference on Lasers and Electro Optics/Quantum Electronics and Laser Science Conferences, Anaheim, California, June 2-7, 1996.

118. P. Marsh, K. Hong and D. Pavlidis, "InGaAs-Based mm-Wave Integrated Subharmonic Mixer Exhibiting Low Input Power Requirement and Low Noise Characteristics," *Proc. of the 8th International Conference on Indium Phosphide and Related materials*, pp. 57-60, Schwabisch Gmund, Germany, April 21-24, 1996.

119. D. Pavlidis, "Status of Heterostructure Field Effect Transistor Developments," presented at the Workshop on Compound Semiconductor Devices and Integrated Circuits, pp. 106-107, Vilnius, Lithuania, May 19-21, 1996.

120. D. Pavlidis, E. Alekseev, K. Hong and D. Cuik "InP-Based Millimeter-Wave PIN Diodes for Switching and Phase Shifting Applications," presented at the Topical Workshop in Heterostructure Microelectronics (TWHM 96), Sapporo, Japan, August 18-21, 1996.

121. E. Alekseev, D. Pavlidis and T. Hackbarth, "W-Band InGaAs/InP PIN Diode Monolithic Integrated Switches," presented at the GaAs International Conference, pp. 285-288, Orlando, Florida, November 3-6, 1996.

122. D. Sawdai, J-O. Plouchart, D. Pavlidis, A. Samelis and K. Hong, "Power Performance of InGaAs/InP Single HBT's," *Proc. of 8th International Conference on Indium Phosphide and Related Materials*, pp. 133-136, Schwabisch Gmund, Germany, April 21-24, 1996.

123. D. Pavlidis and K. Hong, "Low-Leakage Buffers for MOCVD Grown InAlAs/InGaAs HEMTs," presented at the Workshop on Compound Semiconductor Devices and Integrated Circuits, pp. 28-29, Vilnius, Lithuania, May 19-21, 1996.

124. J. Ch. Garcia, C. Dua, S. Mohammadi and D. Pavlidis, "Hydride- Free Chemical Beam Epitaxy Processes and Application to GaInP/GaAs Heterojunction Bipolar Transistors," presented at the 38th Electronic Materials Conference, Santa Barbara, California, June, 1996.

125. K. Kamath, P. Bhattacharya and J. Phillips, "Room Temperature Luminescence from Self-Organized $In_xGa_{1-x}As/GaAs$ ($0.35<x<0.45$) Quantum Dots with High Size Uniformity," presented at the 9th International Conference on Molecular Beam Epitaxy, Malibu, California, August, 1996.

126. K. Zhang, K. Kamath, J. Singh and P. Bhattacharya, "Bandgap Modulation and Quantum Wire Formation in Dielectric Strip-Loaded Quantum Wells," presented at the Electronic Materials Conference, Santa Barbara, California, June, 1996.

127. K. Kamath, J. Phillips, T. Sosnowski, X. Zhang, T. Norris and P. Bhattacharya, "Room Temperature Operation of MBE Self-Organized InGaAs Quantum Dot Lasers," presented at the Fifteenth International Semiconductor Laser Conference, Haifa, Israel, October, 1996.

128. J. Phillips, K. Kamath, T. Sosnowski, T. Norris and P. Bhattacharya, "Room-Temperature Luminescence 1 μm Junction Laser Operation of $In_xGa_{1-x}As/GaAs$ Quantum Boxes Formed by Self-Organized Molecular Beam Epitaxy," presented at the IEEE Lasers and Electro-Optics Society Annual Meeting, Boston, Massachusetts, November, 1996.

129. K. Kamath, P. Bhattacharya and J. Singh, "Multispectral InGaAs/GaAs/AlGaAs Laser Arrays by MBE Growth on Patterned Substrates," presented at the 9th International Conference on Molecular Beam Epitaxy, Malibu, California, August, 1996.

130. P. Bhattacharya, X. Zhang, Y. Yuan, A. Gutierrez-Aitken, C. Caneau and R. Bhat, "GaAs/InGaAs/AlGaAs (λ=0.98μm) MQW Tunneling Injection Lasers with 84 GHz Intrinsic Modulation Bandwidth Grown by MOVPE," presented at the International Conference on Metalorganic Vapor Phase Epitaxy, Cardiff, UK, June, 1996.

131. X. Zhang, Y. Yuan, A. Gutierrez-Aitken, P. Bhattacharya, C. Caneau and R. Bhat, "MQW Tunneling Injection Lasers (λ=.98μM) with 84 GHz Intrinsic Modulation Bandwidth," presented at the 54th Device Research Conference, Santa Barbara, California, June, 1996.

132. P. Bhattacharya, X. Zhang, Y. Yuan, A. Gutierrez-Aitken, C. Caneau and R. Bhat, "Tunneling Injection Lasers with K=0.105ns and 84 GHz Intrinsic Modulation Bandwidth," presented at the Conference on High Speed Optoelectronics Devices and Systems, Snowbird, Utah, August, 1996.

133. X. Zhang, Y. Yuan, A. Gutierrez-Aitken and P. Bhattacharya, "0.98 μm Multiple Quantum Well Tunneling Injection Lasers with 84 GHz Intrinsic Modulation Bandwidth," presented at the Fifteenth International Semiconductor Laser Conference, Haifa, Israel, October, 1996.

134. H. Jiang and J. Singh, "Calculations of Strain Distribution and Electronic Spectra in Self-Assembled Semiconductor Quantum Dots," presented at the American Physical Society Meeting, Kansas City, March, 1997.

135. H. Jiang, J. M. Hinckley and J. Singh, "Hot Carrier Dynamics in Silicon Through Free Carrier Absorption: A Theoretical Model," presented at the American Physical Society Meeting, Kansas City, March, 1997.

136. K. Yang, G. Munns, X. Wang and G. Haddad, "Double Heterojunction Bipolar Transistors with Chirped InGaAs/InP Superlattice Base-Collector Junction Grown by CBE," presented at the 9th International Conference on InP and Related Materials (IPRM), Cape Code, Massachusetts, pp. 645-648, May 11-15, 1997

137. K. Yang, G. O. Munns, J. R. East and G. I. Haddad, "InP Double Heterojunction Bipolar Transistors with Chirped InGaAs/InP Superlattice Base-Collector Junction Grown by CBE," presented at the 1997 IEEE Cornell Conference, pp. 278-286, August 4-6, 1997.

138. K. C. Syao, K. Yang, A. L. Gutierrez-Aitken, X. Zhang, G. Haddad and P. Bhattacharya, "16-Channel Monolithically Integrated InP-Based p-i-n/HBT Photoreceiver Array with 11-GHz Channel Bandwidth and Low Crosstalk," presented at the Conference on Optical Fiber Communication, OFC'97, Dallas, Texas, pp. 15-16, February 16-21, 1997.

139. J. P. Sun, H. B. Teng, G. Haddad, M. Stroscio and G. Iafrate, "Intersubband Relaxation in Step Quantum Well Structures," presented at the International Workshop on Computational Electronics, Notre Dame, Indiana, May 28-30, 1997.

140. J. P. Sun, H. B. Teng, G. I. Haddad and M. Stroscio, "Electron- interface Phonon Interaction in Multiple Quantum Well Structures," presented at the Devices Workshop, Maui, Hawaii, December 8-12, 1997.

141. H. Gebretsadik, K. Kamath, K. Linder and P. Bhattacharya, "Growth and Characterization of Defect-Free GaAs/AlAs Distributed Bragg Reflector Mirrors on Patterned InP-Based Heterostructures and VCSELs," presented at the 16th North American Conference on Molecular Beam Epitaxy, May, 1997

142. D. Klotzkin, K. Kamath, R. Jambunathan and P. Bhattacharya, "DC, Modulation and Gain-Switched Characteristics of Self-Organized $In_{0.4}Ga_{0.6}As/GaAs$ Quantum Dot Room Temperature Lasers," presented at the National Electron Devices Meeting, Washington, D.C., December 7-10, 1997.

143. P. Goetz, H. Eisele, K. Syao and P. Bhattacharya, "1.55μm p-i-n/HBT Photoreceiver in a High-Frequency Optical Phase-Locked Loop for Stable Dense Wavelength Division Multiplexing Channel Offsets," presented at the IEEE/LEOS'97 Lasers and Electro-Optics Society Meeting, San Francisco, California, November 10-13, 1997.

144. K. Syao, K. Yang, A. Gutierrez-Aitken and P. Bhattacharya, "Single and Multi-Channel 1.55μm Monolithically Integrated Photoreceivers," presented at the 1997 International Semiconductor Device Research Symposium, Charlottesville, Virginia, December 10-13, 1997.

145. J. W. Park, D. Pavlidis, S. Mohammadi, C. Dua and J. Garcia, "Improved High Frequency performance by Composite Emitter AlGaAs/GaInP Heterojunction Bipolar Transistors Fabricated Using Chemical Beam Epitaxy," presented at the 24th International Symposium on Compound Semiconductors, ISCS'97, San Diego, California, September 7-11, 1997.

146. A. Sibai, F. Ducroquet, K. Hong, D. Cui and D. Pavlidis, "Fourier Transform Infrared Spectroscopy (FTIR), SIMS and Raman Scattering Analysis of Heavily Carbon Doped MOCVD Grown $In_{0.5}Ga_{0.47}As$," presented at the 24th International Symposium on Compound Semiconductors, ISCS'97, San Diego, CA, September 7-11, 1997.

147. Y. Baltagi, C. Bru-Chevallier, G. Guillot, K. Hong and D. Pavlidis, "Impact of Growth Interruption on Interface Roughness of MOCVD Grown InGaAs/InAlAs Studied by Photoreflectance Spectroscopy," presented at the 24th International Symposium on Compound Semiconductors, ISCS'97, San Diego, CA, September 7-11, 1997.

148. P. March and D. Pavlidis, "Noise Analysis of InGaAs Mixer Diodes at Millimeterwave and FAR-Infrared Frequencies," presented at the Workshop on Compound

Semiconductor Devices and Integrated Circuits, (WOCSDICE '97), Scheveningen, The Netherlands, May 25-28, 1997, pp. 67-68.

149. T. Abbott-Morse, T. Brock, J. East and G. Haddad, "Design, Fabrication and Evaluation of Deep Submicron FET's," presented at the IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, New York, August, 1997.

150. P. Bhattacharya, K. Syao and A. Gutierrez-Aitken, "1.55μm InP-Based Monolithically Integrated Multi-channel Photoreceiver Arrays," presented at Photonics West, San Jose, California, January 24-30, 1998.

151. J. Phillips, K. Kamath and P. Bhattacharya, "InAs/GaAs Self- Organized Quantum Dot Far-Infrared Detectors," presented at the 1998 Conference on Lasers and Electro-Optics, San Francisco, California, May 3-8, 1998.

152. C. H. Lin, K. Yang, M. Bhattacharya, X. Zhang, J. R. East, P. Mazumder and G. I. Haddad, "Monolithically Integrated InP-Based Minority Logic Gate Using an RTD/HBT Heterostructure," presented at IPRM'98, Tsukuba, Japan, May 11-15, 1998.

153. E. Berg and S. Pang, "Comparisons Between Electrical and Optical Characteristics of Etch Induced Damage in InGaAs," presented at the International Conference on Electron, Ion and Phonon Beam Technology and Nanofabrication, May, 1998.

154. D. Pavlidis, "Metalorganic Chemical Vapor Deposition (MOCVD) Material Growth and Application to InP-Based Electronic Devices," *Proc. of IEEE International Conference on Indium Phosphide and Related Materials,* Tsukuba, Japan, May 11-15, 1998, pp. 477-480.

155. J. Park, S. Mohammadi and D. Pavlidis, "GaInP/GaAs HBT Technology Using TBA, TBP Precursors and Application to Optoelectronic Circuits," presented at 22nd Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDIC 98), Zeuthen, Germany, May 24-27, 1998, pp. 33-34.

156. J. W. Park, S. Mohammadi, D. P. C. Dua and J. C. Garcia, "GaInP/GaAs HBT Broadband Monolithic Transimpedance Amplifier and their High Frequency Small and Large Signal Characteristics, Presented at the IEEE MTT-S International Microwave Symposium, Baltimore, MD, June 7-9, 1998.

157. E. Alekseev, D. Cui and D. Pavlidis, "Power-Handling Capability of W-Band InGaAs Pin Diode Switches," Proceedings of the IEEE International Conference on Indium Phosphide and Related Materials (IEEE-IPRM 98), Tsukuba, Japan, pp. 199-202, May 11-15, 1998.

158. E. Alekseev, D. Pavlidis and C. Tsironis, "W-Band On-Wafer Load- Pull Measurement System and Its Application to HEMT Characterization," Presented at the IEEE MTT-S International Microwave Symposium, Baltimore, MD, June 7-9, 1998.

159. J. Papapolymerou, J. East, L. Katehi, M. Kim and I. Mehdi, "Millimeter-Wave GaAs Monolithic Multipliers," presented at The International Microwave Symposium, Baltimore, Maryland, June, 1998.

160. P. Goetz, H. Eisele, K. Syao, K. Yang and P. Bhattacharya, "InP-Based Gilbert Cell Phase Detector for Generation of Stable Dense Wavelength Division Multiplexing Channel Offsets Using an Optical Phase-Locked Loop, presented at The International Microwave Symposium, Baltimore, Maryland, June, 1998.

7.2 SCIENTIFIC PERSONNEL SUPPORTED BY THIS PROJECT AND DEGREES AWARDED DURING THIS REPORTING PERIOD:

Total Number of Ph.D. Graduates: 31
Students who received a Ph.D. degree during this program:

Student	Advisor
T. Abbott Morse	G. Haddad
F. Brauchler	G. Haddad
W. L. Chen	G. Haddad
J. Cowles	G. Haddad
A. Gutierrez-Aitken	P. Bhattacharya
K. Eisenbeiser	G. Haddad
P. Goetz	P. Bhattacharya
K. Hong	D. Pavldis
M. Karakucuk	G. Haddad
D. Klotzkin	P. Bhattacharya
K. Ko	S. Pang
Y. Kwon	D. Pavlidis
P. Marsh	D. Pavlidis
S. Mohan	P. Mazumder
K. Moore	G. Haddad
D. Nichols	P. Bhattacharya
S. Peng	G. Haddad
D. Pehlke	D. Pavlidis
A. Samelis	D. Pavlidis
V. Sankaran	J. Singh
D. Sawdai	D. Pavlidis
H. C. Sun	P. Bhattacharya
J. P. Sun	G. Haddad
C. Y. Sung	T. Norris
K. Syao	P. Bhattacharya
D. Teeter	G. Haddad
M. Tutt	D. Pavlidis
I. Vurgaftman	J. Singh
K .Yang	G. Haddad
K. Yeom	J. Singh
H. Yoon	P. Bhattacharya

7.3 INTERACTIONS WITH ARMY LABORATORIES

Date	Individual/Group	Purpose/Interaction
10/92	Profs. G. I. Haddad, P. Bhattacharya J. Singh R. Brown D. Pavlidis	A ECOG Meeting was hosted by the University and presentations were given on current research work. In attendance were: B. Ahn, A. Ballato, H. Berger, H. Everitt, J. Ferrick, D. Heminway, J. Kohn, E. Kunhardt, W. Martin, J. Mink, M. Pastel, B. Perlman, T. Reader, W. Sander, J. Sattler, F. Schwering, J. Shappirio, H. Soicher D. Smith, M. Stroscio, R. Trew, R. Voss and J. Zavada.
3/9/93	Prof. G. Haddad	Made a presentation on URI research activities to the U.S. Army Research Laboratory, Electronics and Power Sources Directorate, and interacted with several individuals and groups, including Drs. Thornton, Tompsett, Jones, Perlman, etc.
4/13/93	Prof. G. Haddad	Visited ARO and participated in a review of the externally sponsored research programs.
5/26/93	Profs. Haddad, P. Bhattacharya, J. Singh, D. Pavlidis, P. Mazumder, F. Terry, and S. Pang	URI Review. Presentations on various aspects of research were presented by faculty. In attendance were from ARO: M. Stroscio, U. S. Army Night Vision and Electro-Optics Laboratory: J. Pollard, U. S. Army Missile Command: R. Lane, U. S. Army Space and Strategic Defense Command: W. Martin, U. S. Army, Fort Monmouth: M. Tompsett, W. Chang and B. Perlman, ARL-HDL: M. Tobin, ONR: L. Cooper, AFOSR-WPAL: G. McCoy, C. Huang, R. Lee, J. Loehr and C. Bozada, and AFOSR-BAFB: G. Witt

Date	Individual/Group	Purpose/Interaction
6/2/93	Prof. S. Pang	Presented a talk entitled "Low Damage and High Precision Dry Etching Using an Electron Cyclotron Resonance Source" at the Dry Etching Workshop, Army Research Laboratories.
6/23/93 - 6/25/93	Prof. G. Haddad	Visited the U.S. Army Research Laboratory, Electronics and Power Sources Directorate and participated in a review of the inhouse research programs being carried out.
9/29/93	Prof. G. Haddad	Made a presentation at the Joint Meeting of the Executive Advisory Boards for the U.S. Army University Research Initiative Centers, Fort Monmouth, New Jersey.
10/25/93	Prof. G. Haddad	Met with Dr. C. Thornton in Ann Arbor, Michigan, to discuss cooperative efforts with the Electronic Devices Research Division of the Army Research Center.
5/94	Profs. Haddad, P. Bhattacharya, P. Mazumder, S. Pang, D. Pavlidis and J. Singh	URI Review. Presentations on various aspects of research were presented by faculty. In attendance were from ARO: J. Harvey, M. Stroscio, M. Littlejohn, J. Mink; ARL: H.-L. Cui, E. Lenzing, A. Lepore, B. Perlman; U. S. Army Space and Strategic Defense Command: W. Martin; Wright-Patterson AFB: G. McCoy; Bellcore: C. Brackett; AFOSR: G. Witt; Hughes Research Lab: P. Greiling; ONR: L. Cooper; U. Illinois: S. Bishop; TI: W. Wisseman.
11/3/94 - 11/4/94	Profs. G. Haddad, D. Pavlidis and J. Singh	Organized and gave a series of lectures for a training seminar at MICOM, Huntsville, Alabama. Dr. Bill Pittman was the co-organizer.

Date	Individual/Group	Purpose/Interaction
5/95	Profs. G. I. Haddad, P. Bhattacharya, P. Mazumder, S. Pang, D. Pavlidis and J. Singh	URI Review. Presentations on various aspects of research were presented by faculty. In attendance were from ARO: C. Church, J. Harvey, M. Stroscio; ARL: L. Didomenico, A. Lepore, B. Perlman, M. Tobin; U. S. Army Space and Strategic Defense Command: W. Martin, R. Rodgers; ONR: L. Cooper; U. Illinois: S. Bishop; Hughes Research Lab: P. Greiling; Boeing Company: C. S. Hong; U.S. Military Academy: G. Tait, B. Tousley; TI: W. Wisseman.
10/95	Profs. G. I. Haddad, P. Bhattacharya, M. Elta, M. Islam, L. Katehi, P. Mazumder, G. Mourou, C. Nguyen, S. Pang, D. Pavlidis, G. Rebeiz, J. Singh, F. Ulaby and K. Wise	A ECOG Meeting was hosted by the University and presentations were given on current research work. In attendance were: B. Ahn, C. Church, W. Cunningham, J. Fleischman, J. Harvey, J. Kohn, R. Mihailovich, B. Perlman, E. Poindexter, R. Rodgers, W. Sander, M. Stroscio, S. Svensson, D.-W. Tu, J. Zavada and R. McClelland
10/95	Prof. G. I. Haddad	Visited the U.S. Army Tank Automotive Command in Detroit, Michigan to get acquainted with their research program and try to develop close interactions with them.
5/96	Profs. G. I. Haddad, P. Bhattacharya, L. Katehi, P. Mazumder, S. Pang, D. Pavlidis and J. Singh	URI Review. Presentations on various aspects of research were presented by faculty. In attendance were from ARO: H. Everett, B. Guenther, J. Harvey, M. Stroscio, R. Trew; ARL: G. Borsuk, B. Perlman, E. Potenziani, S. Svenssen; Wright Laboratory: M. Estes; U. Illinois: S. Bishop; Hughes Research Lab: P. Greiling; Boeing Company: L. Figueroa; U.S. Military Academy: A. Sayles; TI: W. Wisseman.

Joint Publications and Research with Army Scientists

1. J. Pamulapati, P. K. Bhattacharya, R. L. Tober, J. P. Loehr and J. Singh, "Characterization of High-Quality Pseudomorphic InGaAs/GaAs Quantum Wells by Luminescence and Reflectance Techniques," *Journal of Applied Physics*, **71**, 4487 (1992).

2. R. L. Tober, W. Q. Li and P. K. Bhattacharya, "Confinement Effects on Electroreflectance Spectra," Presented at the SPIE's 1992 Symposium on Compound Semiconductor Physics and Devices, Somerset, NJ, March 1992.

3. R. L. Tober, W. Q. Li and P. K. Bhattacharya, "Differential Photocurrent Spectroscopy Using Novel Characterization Techniques," *Journal of Applied Physics*, **71**, 3506, (1992).

4. R. Tober, T. Bahder, W-Q. Li and P. Bhattacharya, "Optically Induced Energy Shifts of Excitonic Resonances in Single [111]B and [100] InGaAs Quantum Wells", presented at the Electronics Materials Conference, Cambridge, MA, June 1992.

5. SeGi Yu, K. W. Kim, M. A. Stroscio, G. J. Iafrate, J. P. Sun and G. I. Haddad, "Transfer Matrix Technique for Interface Optical Phonon Modes in Multiple Interface Heterostructure Systems," *J. Appl. Phys.*, **82**, 3363-3367, 1997.

6. J. P. Sun, H. B. Teng, H. I. Haddad, M. Stroscio and G. J. Iafrate, "Intersubband Relaxation in Step Quantum Well Structures," *VLSI Design*, to appear, 1998.

7. J. P. Sun, H. Teng, G. I. Haddad, and M. Stroscio, "Electron-Interface Phonon Interaction in Multiple Quantum Well Structures," *Semiconductor Science and Technology*, to appear, 1998.

Other Interactions

- University of Michigan has supplied III-V semiconductor layers to ARL scientists.
- University of Michigan has supplied MBE grown metallic films on III-V Compounds to ARL scientists for Schottky-Barrier characterization.
- Discussions with Drs. M. Tobin and G. Simonis at ARL on picosecond measurements on high-speed detectors and integrated devices. Devices were provided to Dr. Simonis for optical Heterodyning measurements and to Drs. Pamulapati and Dutta for characterization.
- Collaboration with Dr. Ken Jones of ARL on the study of growth of epitaxial ohmic contacts on GaAs and on shallow ohmic contacts.
- Consulted with Dr. Tobin and her group at ARL on MOMBE systems.
- Consulted with Dr. R. Lane of MICOM on device technology for radar systems.
- One of the students working on this project (Doug Teeter) spent the summer working at the U.S. Army Electronics Command at Fort Monmouth on large signal device modeling and characterization. The contact person is Dr. Barry Perlman.
- Discussions with M. Stroscio about modular upgrades to defense systems. These discussions were prompted by inquiry from the Tactical Operations Office at the Pentagon.

- Discussions were held with R. Lane, Army Missile Command relevant to the GaAs processors.
- Supplied MBE layers to Dr. R. Tober of HDL and continued interactions relative to piezoelectric measurements on layered structures.
- Discussions were carried out with Dr. M. Stroscio on the scattering processes for carrier relaxation in quantum wire structures and polarization dependent measurements.
- The main experimental portion of the project entitled "Heterojunction Bipolar Transistor Modeling, Design, Fabrication and Evaluation" is large signal characterization of devices. We have obtained devices from Texas Instruments with the help of Dr. Ali Khatibzadeh and from Raytheon Research Division with the help of Dr. Michael Alderstein. Dr. Douglas Teeter, a former student on the project, is now at Raytheon Research Division. We are planning to combine our efforts for the pulsed measurements discussed in section V of this report. We have also started working with Dr. Martin Herman of NASA/JPL on characterization of power amplifiers for space applications. The HBT work at Raytheon and Texas Instruments is funded by Marko Afendykiw for the Naval Weapons Center at China Lake. We are also working with Drs. Larry Larson and Paul Greiling at Hughes Research Laboratory and Dr. Tim Drummond at Sandia laboratory.
- Noise measurements on small signal devices were done at Wright Patterson Air Force Base.
- Organized and gave most of the lectures for intensive short courses on millimeter wave devices and circuits for the U. S. Army Missile Command.
- A joint research program to study basic properties of ohmic contacts and Schottky barriers has been initiated with K. Jones of Army Research Laboratory and Jack East as collaborator.
- A joint research program was initiated and collaborative work continues to study the defects induced by dry etching, with Dr. M. W. Cole of the Army Research Laboratory Electronics Division (Surface Analysis Group) in collaboration with Prof. Pang.
- Photoreflectance measurements on quantum wires and dots were performed by Dr. R. Tober at Army Research Laboratory.
- Prof. Pang has joint projects with Naval Research Laboratory and NIST to analyze surface defects using photoreflectance and study surface passivation.
- A joint program with Hughes Research Laboratory to develop controllable etch process for HBTs with Prof. Pang.
- Joint development work with Wavemat Inc. on the optimization of etch uniformity and development of automatic tuning of ECR cavity with Prof. Pang.
- Prof. Pang is collaborating with Plasma Therm Inc. on inductively coupled plasma source.
- Prof. Pang has joint projects with GM research laboratory on anisotropic etching of thick polymer and Si layers, with Ford Motor Co. on high aspect ratio etching of Si channels, with TI to develop fast etching for III-V based devices, with TRW to develop deep via hole etching for InP-based MMIC, and with Advanced Photonix to develop deep Si channels for imaging arrays.

- A joint program with Draper Laboratory to develop resonate based microsensors with Prof. Pang.
- Prof. Haddad and Dr. J. P. Sun are cooperating with Drs. Stroscio and Iafrate on modeling of quantum wells and their applications.
- Prof. Bhattacharya consulted with Drs. J. Pamulapati, K. Choi and M. Dutta from ARL.
- Prof. Haddad serves on the NRC Technical Advisory Board for ARL.

7.4 INTERACTIONS WITH OTHER D.O.D. FEDERAL AND INDUSTRIAL AGENCIES AND LABORATORIES

This program has had a major impact in establishing Michigan as one of the leading centers in III-V semiconductor technology and high-frequency/speed microelectronics and optoelectronics. This has lead to the establishment of very close interactions with and initiation of several major programs and centers from various federal and industrial organizations. These include:

- The NASA Center for Space Terahertz Technology. Through this Center we have established very close interactions with JPL and Goddard.
- The NSF-Science and Technology Center for Ultrafast Optics.
- The SRC Center for Automated Semiconductor Manufacturing.
- ARPA: Several major programs in GaAs microprocess design and fabrication (joint with several companies and monitored by Army Research Office), automated III-V semiconductor manufacturing (joint with Hughes Research Laboratories), novel superlattice-based HBT devices for optically controlled phased-array radar applications (monitored by the Air Force-Rome Center), resonant tunneling devices for ultralight speed and dense digital circuits (ARPA-monitored by ARO). A program on HBT circuit design with Texas Instruments and Cadence design systems, and a new Center on Optoelectronic Science and Technology with Illinois, Texas and several companies.
- ONR: Programs in basic material growth studies, high-speed optoelectronic devices and wide bandgap semiconductors.
- AFOSR: Programs in Si/Ge materials technology and III-V optoelectronic devices for optical computing. A MURI-program in automated electronics manufacturing and control.
- Industry: Several programs and very close interactions with Hughes, Texas Instruments, Northern Telecom, Ford Motor Co., Plasma Therm Inc., IBM, National Semiconductor, Hewlett-Packard, MACOM, INSA-LYON, Daimler Benz, Ecole Centrale de Lyon, Rockwell, Alcatel, Bellcore Laboratories, Lasertron, Raytheon, Lockheed-Martin, AT&T, Westinghouse, Thomson-CSF, Focus, Allied-Signal, ERIM, the Mayo Clinic, U. of Texas at Dallas, Arizona State University, U. of Illinois at Urbana, and others.
- NSF: Several programs in material growth and characterization and optoelectronic devices and a recent program for curriculum-research developed in automated semiconductor manufacturing.

- State of Michigan: A Center for Display Technology and Manufacturing which involves many companies.
- ARO-MURI Program in Low Power/Low Noise Electronics for Communication Systems.
- ARO-MURI Program on Low-Energy Electronics Design for Mobile Platforms.
- ARO-MURI Program on an Adaptive Optoelectronic Eye.

RESEARCH

RESEARCH TASKS

I. ELECTRONIC, OPTICAL AND TRANSPORT PROPERTIES IN HETEROSTRUCTURE BASED DEVICES

FACULTY SUPERVISOR: J. Singh

RESEARCH STAFF: Dr. John M. Hinckley

GRADUATE STUDENT PARTICIPANTS: H. Jiang
Y. Lam
I. Vurgaftman
K. Yeom

PERIOD: July 1, 1992 - June 30, 1998

TASK OBJECTIVES:

The objective of our task was to understand the electronic bandstructure, optical response and transport properties in semiconductor heterostructures. Once this understanding was established it was our goal to exploit it to design electronic and optoelectronic devices with superior performance.

MAJOR ACCOMPLISHMENTS:

The following is a list of our major accomplishments.

- *Carrier Thermalization in Heterostructures and its Link to High Frequency Operation of Semiconductor Lasers – A Proposal for Tunneling Injection Lasers:* An important question that had puzzled scientists for a number of years was "why is it that electronic devices can operate at frequencies as high as 300 GHz, but semiconductor lasers can barely go over 30GHz?" To shed light on this question we performed the first Monte Carlo calculations for carrier injection and thermalization in quantum well lasers. Our studies clearly showed that while carrier thermalization times in bulk semiconductors were ~1 ps, in quantum wells these times were ~10-20 ps. The influence of this long carrier thermalization time on laser dynamics was studied by us. We showed that the slower carrier relaxation times would limit the performance of quantum well lasers ~50-60 GHz even under the best conditions. To circumvent this long relaxation time we proposed the tunneling injection laser. In this structure carrier thermalization in a wide layer and then tunnel into the active quantum well region for lasing. This idea was demonstrated by Prof. Bhattacharya's group and is now an active area of research in laser physics.

- *Microcavity Structures and Thresholdless Lasing:* We have theoretically examined the photon modes in microcavity structures where confinement dimensions approach the wavelength of light. The singularity in the photon density of states have been shown by us to lead to laser designs with essentially thresholdless lasers.

- *Strain in MODFETs and Breakdowns:* We have carried out theoretical studies on how strain in a semiconductor layer influences the breakdown properties of devices. We have shown that compressive strain can greatly enhance the breakdown properties by increasing the threshold energy for onset of avalanche breakdown. This effect was observed in Prof. Haddads group and several other groups around the world.

- *Intersubband Effects in Quantum Dots:* We have calculated the intersubband scattering rates in quantum dots. For properly designed quantum dot structures these times can become quite long since electron- phonon interaction becomes ineffective. Such quantum dot structures can be used to design temperature independent intersubband devices. Examples include long wavelength lasers and detectors. We have calculated many of the important design properties of these devices.

WORK PERFORMED:

The following areas were addressed during this five-year period.

- *Bandstructure of Heterostructures:* We have developed k·p and tight binding formalisms to study bandstructure of i) quantum wells for lasers. This includes strained quantum well lasers; ii) quantum wires and quantum dots. We have applied an 8 band k·p model to study the bandstructure of self-assembled quantum dots.

- *Scattering Rates in Low Dimensional Systems:* We have calculated in detail all the important scattering mechanisms in quantum wells, quantum wires, and quantum dot structures. We have shown that the electron-phonon scattering rates are suppressed in quantum wires and dots and how these can lead to novel devices.

- *High Speed Laser Limitations:* We have done Monte Carlo simulated to examine the laser frequency limits in quantum well, quantum wire and quantum dot lasers. We have calculated gain compression factors and shown how carrier thermalization times influence laser high frequency operation.

  We have also examined how laser frequency can be improved by the tunneling injection laser in which carriers are thermalized in a wide region in subpicosecond times and then injected by tunneling into the active region.

- *Semiconductor Device Breakdown Studies:* We have used full bandstructure Monte Carlo methods to examine breakdown in Si, Ge, SiGe alloys, InGaAs systems. Both strained and unstrained materials have been examined. we have shown that the presence of biaxial strain suppresses electron initiated impact ionization rates.

  We have also examined the breakdown of semiconductors by intense laser pulses. We have calculated how the ac breakdown field relates to the dc breakdown fields.

PUBLICATIONS:

No new publications since last report, January, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

II. QUANTUM TRANSPORT MODELING OF RESONANT-TUNNELING STRUCTURES AND DEVICE APPLICATIONS

FACULTY SUPERVISOR: G. I. Haddad

RESEARCH STAFF: J. P. Sun and R. Mains

GRADUATE STUDENT PARTICIPANTS Hongbo Teng
J. P. Sun

PERIOD: July 1, 1992 - June 30, 1998

TASK OBJECTIVES:

The objective was to develop quantum transport formalisms and simulation programs to predict the behavior of quantum devices. The modeling capabilities developed was employed in understanding and design of novel quantum devices under study and development in the research program.

WORK PERFORMED:

1. Computer programs for modeling and simulation of resonant tunneling devices were developed.
2. Device simulations for theoretical studies and design calculations of various kinds of quantum devices were performed.
3. More than 10 research papers and conference presentations related to the quantum modeling work were published or presented during this period.

MAJOR ACCOMPLISHMENTS:

1. Proposed and demonstrated a novel quantum device: the quantum well varactor, in which triple quantum barriers and double quantum wells were incorporated. Our self-consistent quantum model was employed to conceive and design the device structure and to simulate its C-V and I-V characteristics. Record peak-to-valley capacitance ratio was demonstrated experimentally, in very good agreement with modeling predictions. Similar results were also achieved on quantum varactors with superlattice structures.

2. A quantum model for hot electron transistors was developed and used for study of ballistic transport and energy spectrum of electrons in hot electron devices, in good agreement with our experimental data.

3. Developed a self-consistent quantum model of Γ-X mixing effects in quantum well structures. The quantum transmitting boundary method was implemented in these calculations.

4. An accurate re-formulation of the Wigner function method for quantum transport modeling was developed and implemented for calculations of I-V characteristics of resonant tunneling diodes.

5. A formalism derived from the optical model in neutron scattering theory was developed and implemented for scattering calculations in modeling realistic resonant tunneling devices. Very good agreement with experimental I-V characteristics was obtained. Furthermore, self-consistency, transverse momentum, and phonon scattering were incorporated in a unified formulation.

6. Our quantum models of resonant tunneling diodes and transistors were used to extract parameters for circuit models of these quantum devices. The results have been used and implemented in development of NDR- SPICE (Negative Differential Resistance SPICE), an enhanced version of *spice-3e* program for logic circuit design simulations.

7. We participated in the evaluation of the nationwide nanoelectronic modeling program (NEMO) and performed extensive work in testing and evaluation of NEMO software. A part of this work was summarized in a comprehensive review article on quantum device modeling published in the Proceedings of the IEEE, April 1998.

8. Developed quantum formulations and simulation programs for laser structures based on quantum wells, which aided research on quantum well lasers. See Part VII for more description and a list of publications in this area.

PUBLICATIONS:

1. J. P. Sun, G. I. Haddad, P. Mazumder and J. N Schulman, "Resonant Tunneling Diodes: Models and Properties," *Proceedings of the IEEE*, **86**, 641-661, April 1998.

2. P. Mazumder, S. Kulkarni, M. Bhattacharya, J. P. Sun and G. I. Haddad, "Digital Circuit Applications of Resonant Tunneling Devices," *Proceedings of the IEEE*, **86**, 664-686, 1998.

Ph.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

INTERACTIONS WITH ARMY LABORATORIES:

Close collaboration and many technical discussions with Dr. Michael Stroscio of Army Research Office on quantum transport theories. in quantum well structures.

INTERACTIONS WITH INDUSTRIES AND UNIVERSITIES:

Close collaboration with the NEMO team, Texas Instruments, on NEMO evaluations; Many technical discussions with Dr. J. N. Schulman, of Hugh Research Labs; Technical discussions with Dr. H. L. Grubin of Scientific Research Associates, Dr. W. Frensley of University of Texas at Dallas, and Dr. D. K. Ferry of Arizona State University.

III. HETEROJUNCTION BIPOLAR TRANSISTOR MODELING, DESIGN, FABRICATION AND EVALUATION

FACULTY SUPERVISOR: G. I. Haddad

RESEARCH SCIENTIST: K. Yang

GRADUATE STUDENT PARTICIPANTS: J. Cowles
K. Yang
G. Munns
J. Kempf

PERIOD: July 1, 1992 - June 30, 1998

TASK OBJECTIVES:

The major objectives of this task were to model, design, fabricate and characterize heterojunction bipolar transistors (HBT's) based on III-V compound- semiconductor material systems, which are possibly grown with CBE and MBE growth systems. These devices will be used in high-speed digital and optoelectronic integrated circuits, and micro/millimeter-wave power applications.

MAJOR ACCOMPLISHMENTS:

- A numerical model, in which the coupled transport processes of drift-diffusion and tunneling-thermionic emission across an abrupt heterojunction are taken into account for the first time in a single coupled formulation, has been developed. This model was used to study the performance of GaAs- and InP-based HBT's.
- InP/InGaAs single HBT's (SHBT's), whose layer structure has been optimized for high-speed p-i-n/HBT shared-layer OEIC photoreceivers, demonstrated excellent high-frequency performance, characterized by maximum cutoff frequencies of f_t = 105 GHz and f_{max} = 160 GHz. The designed and fabricated high-speed p-i-n/HBT photoreceiver demonstrated a record high bandwidth of 19.5 GHz with a transimpedance gain of 46 dBΩ for an OEIC front-end photoreceiver. These results are discussed in detail in the Section of *Design, Modeling and Characterization of High-speed InP-Based OEIC p-i-n/HBT Photoreceivers.*

- A unified CAD-based HBT model for InP SHBT's has been developed and implemented in HSPICE simulation program. This large-signal model was used for detailed dc, small-signal rf and large-signal transient performance characterization of the devices and related integrated circuits.

- InP-based double HBT's (DHBT's), which are suitable for use in micro-/millimeter-wave power applications, have been designed and grown by CBE. The fabricated DHBT's with an InP/InGaAs chirped-superlattice (CSL) B-C junction demonstrated a high common-emitter breakdown voltage (BV_{CEO}) of 18.3 V with a typical current gain of 55. Maximum cutoff frequencies of f_{max} = 146 GHz and f_T = 71 GHz were obtained from the fabricated DHBT's. The obtained value of f_{max} = 146 GHz is the highest up to date for an InP-based DHBT, which has a BV_{CEO} larger than 18 V.

WORK PERFORMED:

A self-consistent numerical model was developed to understand internal device physics of abrupt heterojunction devices. The model was used to improve the overall performance of HBT's for a number of high-speed applications. The layer structure of an InP-based SHBT has been optimized for use in high-speed long-wavelength (1.55μm) OEIC photoreceiver applications based on a p-i-n/HBT shared-layer integration scheme. The fabricated self-aligned small-emitter HBT's with an InGaAs collector thickness larger than 6000Å showed excellent high-frequency performance. The fabricated devices were tested under dc and small-signal ac operating conditions over a wide bias range. Through detailed characterization of the devices, a unified HSPICE HBT macro model, which is valid over a wide range of operating conditions, has been developed. The model and extracted parameters were used to design and optimize the performance of integrated p-i-n/HBT photoreceiver circuits. Excellent agreement has been achieved between the simulation and experiment. These results will be further described in the Section of *Design, Modeling and Characterization of High-speed InP-Based OEIC p-i-n/HBT Photoreceivers.*

For power micro-/millimeter-wave applications of HBT's, several different InP-based DHBT structures with an InP collector layer have been designed. The design focus has been placed on reducing the carrier blocking effects at the base-collector heterojunction due to the presence of a significant InGaAs/InP conduction-band barrier, while increasing the device breakdown voltage. The InP/InGaAs DHBT heterostructures with a 10-period InGaAs/InP chirped-superlattice (CSL) linear-graded B-C junction were designed and grown by Chemical Beam Epitaxy. The DHBT's were fabricated using our triple-mesa self-aligned emitter- base HBT fabrication technology. The fabricated devices demonstrated large breakdown voltages of BV_{CEO} = 18.3 V and BV_{CBO} = 22.8 V, and high cutoff frequencies of f_{max} = 146 GHz and f_T = 71 GHz. The obtained value of 146 GHz is the highest reported up to date for an InP-based DHBT, which has a breakdown voltage (BV_{CEO}) larger than 18V. The results indicate that the InP-based CSL B-C junction

DHBT's with high f_{max} and large breakdown voltages are very attractive for microwave and millimeter-wave power applications.

PUBLICATIONS:

No new publications since last report, January, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

IV. DESIGN, MODELING AND CHARACTERIZATION OF HIGH-SPEED InP-BASED OEIC p-i-n/HBT PHOTORECEIVERS

FACULTY SUPERVISOR: G. I. Haddad
P. Bhattacharya

RESEARCH SCIENTIST: K. Yang

GRADUATE STUDENT PARTICIPANTS: A. L. Gutierrez-Aitken
K. Yang
J. Cowles
K. C. Syao

PERIOD: July 1, 1992 - June 30, 1998

TASK OBJECTIVES:

The primary objectives of this task were to design, fabricate and evaluate InP-based long-wavelength (1.55μm) monolithic p-i-n/HBT front-end photoreceivers for high-speed optical communication systems. Detailed optoelectronic circuit designs and characterization are conducted with emphasis on low-noise high-speed OEIC performance.

MAJOR ACCOMPLISHMENTS:

- Designed and fabricated high-speed InP-based p-i-n/HBT OEIC photoreceiver demonstrated a measured -3 dB optical bandwidth of 19.5 GHz with a transimpedance gain of 46dBΩ, which is one of the best performance achieved for an InAlAs/InGaAs transimpedance front-end photoreceiver.
- Multi-channel InP-based OEIC photoreceiver arrays for WDM (Wavelength Division Multiplexing) optical communication systems were designed and fabricated using a p-i-n/HBT shared-layer integration scheme. The fabricated 16-channel InP-based OEIC photoreceiver array demonstrated an average channel bandwidth of 11 GHz with a transimpedance gain of 46 dBΩ. The 16-channel photoreceiver is the largest in size and shows the highest bandwidth per channel for any OEIC photoreceiver array to date.

- An InAlAs/InGaAs monolithically integrated photoreceiver array with a novel on-chip shielding, to reduce electrical and optical crosstalk, demonstrated an adjacent-channel crosstalk less than -40 dB, which represents a 17dB reduction compared to -23dB in an array without such shielding.
- Electromagnetic full-wave simulations have been conducted to understand the crosstalk behavior measured from the fabricated OEIC photoreceiver arrays.
- An integrated Darligton amplifier, designed using $5\times5\mu m^2$-emitter self-aligned InP/ InGaAs HBT's, exhibited broadband gain-frequency characteristics from dc to 30 GHz with a gain of 10 dB.

WORK PERFORMED:

The individual active devices and passive elements, which consist of integrated photoreceiver circuits, were fabricated, tested and characterized. Equivalent-circuit models of these devices, including HBT's and p-i-n photodiodes, have been developed and extracted from measured S- parameters and optical-frequency responses. The developed CAD-based device models showed excellent agreement between the measured and simulated results. Based on detailed modeling and characterization of individual devices, high-speed monolithic single-channel and multi-channel photoreceivers were designed and fabricated. Several different transimpedance pre-amplifiers and wideband post-amplifiers were also designed and characterized. The designed and fabricated high-speed single-channel InAlAs/InGaAs p-i-n/HBT OEIC photoreceiver demonstrated a record high -3 dB optical bandwidth of 19.5 GHz for an InAlAs/InGaAs integrated front-end photoreceiver. The measured electrical and optical performance characteristics of fabricated transimpedance amplifiers and OEIC photoreceivers, including small-signal gain-frequency characteristics, transient OEIC response and input-output power characteristics, have been fully characterized using device models implemented in simulation programs of HSPICE and LIBRA. electrical and The OEIC 16-channel p-i-n/HBT photoreceiver arrays, suitable for use in high-capacity WDM transmission links, exhibited a channel bandwidth of 11 GHz with crosstalk less than -23 dB between adjacent channels. The fabricated 16-channel photoreceiver array is the largest in size and shows the highest bandwidth per channel to date for any OEIC photoreceiver array. Photoreceiver arrays based on a novel monolithically integrated radiation-shield design were also fabricated. The radiation shield technique has been found to be very effective in reducing the array crosstalk significantly at high frequencies. The adjacent crosstalk in the radiation-shield OEIC arrays was measured to be less than -35 dB at 10 GHz. These results represent the best performance in multi-channel integrated photoreceiver arrays. An electromagnetic full-wave simulation shows that the measured crosstalk in arrays without the radiation shield could be dominated by radiation crosstalk. The results show that design parameters, such as interchannel spacing and single- or dual-source biasing schemes, are critical to

reduce the crosstalk in monolithic photoreceiver arrays. The details of design, simulation and characterization of the OEIC single- and multi-channel photoreceivers can be found in the papers previously submitted.

PUBLICATIONS:

No new publications since last report, January, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

INTERACTIONS WITH OTHER D.O.D LABORATORIES, INDUSTRIES AND UNIVERSITIES:

AT&T Laboratory Dr. L. Lunardi
Bellcore Laboratories Dr. S. Goswami

V. FET TRANSISTOR MODELING, DESIGN, FABRICATION AND CHARACTERIZATION

FACULTY SUPERVISOR: G. Haddad

RESEARCH SCIENTIST: J. East

GRADUATE STUDENT PARTICIPANTS: T. Abbott
J. Kempf

PERIOD: July 1, 1992 - June 30, 1998

TASK OBJECTIVES:

The major objectives of this task were to model, design, fabricate and RF test FET devices operating above 100 GHz and to better understand the limitations on power and efficiency at lower frequencies.

MAJOR ACCOMPLISHMENTS:

The major work in this project involved the design and characterization of submicron GaAs FET's. A variety of devices were fabricated with gate lengths in the range between 500 and 1000 angstroms. These devices are among the best in the published literature, with f_t values above 100 GHz and f_{max} values above 170 GHz. A detailed experimental investigation of the relationship between process steps such as gate recess etch chemistry and etch depth and the resulting small signal performance were carried out. This study gave a better understanding of the tradeoffs between processing and device performance.

We also developed a large signal, multiple harmonic, time domain measurement system. This system was used to study the large signal nonlinear operation of transistors.

PUBLICATIONS:

No new publications since last report, January, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

INTERACTIONS WITH OTHER D.O.D. LABORATORIES, INDUSTRIES AND UNIVERSITIES:

We have worked with Prof. Milton Feng at The university of Illinois to characterize the noise performance of the FET's fabricated under this project.

VI. HIGH SPEED AND FUNCTIONALITY CIRCUITS BASED ON NEGATIVE DIFFERENTIAL RESISTANCE DEVICES

FACULTY SUPERVISOR: G. I. Haddad
P. Mazumder

RESEARCH SCIENTISTS: J. East
K. Yang

GRADUATE STUDENT PARTICIPANTS: S. Mohan
W. L. Chen
E. Chan
S. Kulkarni
X. Wang

PERIOD: July 1, 1992 - June 30, 1998

TASK OBJECTIVES:

The major objectives of this research were to design and fabricate ultrafast and compact circuits using HBTs and negative differential resistance (NDR) devices such as Resonant Tunneling Transistors (RTTs) and Resonant Tunneling Diodes (RTDs).

WORK PERFORMED:

- **RTD-based logic families:** We have developed a compact, bistable-mode logic family using RTDs in conjunction with HBTs and MODFETs. A binary logic circuit is said to operate in the bistable mode when its output is latched, and any change in the input is reflected in the output only when a clock or other evaluation signal is applied. The bistable mode has been used in several earlier technologies, notably in superconducting logic. The chief disadvantage of these circuits is the requirement of an AC power source whose frequency determines the maximum switching frequency. The logic circuits developed as part of this research use a DC power supply and multiphase clocks but the clock signals are not required to supply large amounts of power as in the case of the earlier circuits. The folded characteristic of the RTD makes it a useful load device which, when properly biased, draws very low currents for both high and low outputs. Resonant tunneling allows picosecond

switching and sharp transitions which result in improved performance of circuits designed using RTDs. For the designed logic family, as long as the clock remains at its quiescent state and the reset signal is not applied, the output does not change with the inputs. However, once the inputs are stable, the correct output can be set by clock evaluation. Hence this circuit operates as a clocked, self-latching threshold element. For a three input circuit, three non-trivial threshold functions can be implemented for the cases where $n = 1, 2, 3$. For $n = 1$, $f1(x_1, x_2, x_3) = 0$ if and only if 1 or more inputs are high. This corresponds to a NOR function. For $n = 3$, $f3(x_1, x_2, x_3) = 0$ if and only if all 3 inputs are high. This corresponds to a NAND function. For $n = 2$, $f2(x_1, x_2, x_3) = 0$ if and only if 2 or more inputs are high. This corresponds to an inverted majority or inverted carry function. Considering the single gate implementation of the carry function, and given the picosecond switching speed of RTD, it is clear that these logic gates can be well used to speed up addition chains, which invariably fall on the critical path in a computing system. This scheme can easily be extended to implement weighted threshold logic elements, by simply assigning different areas to the input transistors. A weighted threshold logic element with m inputs $x_1, x_2, ...x_m$ and weights $w_1, w_2, ...w_m$ has a low output if and only if $w_1x_1 + w_2x_2 + ...w_mx_m > n$ where n is the threshold. It can be seen that the above circuit implements this function when the collector currents of the input transistors are weighted by the factors $w_1, w_2, ...w_m$, and the peak current, I_p, of the RTD is chosen so that the total current through the input transistors exceeds $I_p - I_{clkh}$ exactly when the weighted sum of the logic inputs exceeds the threshold, n. The implementation of the above circuit requires precise control over the RTD and transistor circuits in fabrication. Since the co-integration of RTDs and HBTs is still an active area of research, a prototype version of the above circuit was fabricated. This version 1) places very few constraints on the HBT gain and collector current, as well as the RTD peak and valley currents, and 2) allows the same integrated circuit to be used in testing the functionality of different logic circuits by changing some external voltages. In order to account for possible mismatches between RTD and HBT parameters due to process technology immaturity, large base resistances were used which limit the high-frequency operation of the circuit. The RTDs and HBTs were integrated on the same wafer. The IC was fabricated using CBE-grown InP/InGaAs HBTs and AlAs/InGaAs/AlAs RTDs. Conventional photolithography and lift-off techniques were used to process the active devices and thin-film Ti resistors. The HBTs show maximum DC current gain around 50 and the RTDs have a peak-to- valley current ratio of 6 and peak voltage of 0.3 V. The inverted self-latching MAJORITY gate operated at 1.5 V with an average static current of 3.85 mA, showing a static power consumption of approximately 5.5 mW. The simulated power-delay characteristics of RTD+HBT circuits compare well with the best ECL/CML technologies using silicon or HBT technologies. While this scheme consumes more static power than CMOS circuits, where the static power consumption is zero, it does provide a means to reduce power consumption in high-speed bipolar circuits. When the RTD load was used in an I^2L type of

configuration, total power savings of 50% over conventional HBT I^2L were observed in simulations of divide-by-two frequency dividers. Unloaded gate delays of less than 40 ps were obtained with a power dissipation of 0.4 mW/gate and a logic swing of 0.8 V. In addition, advantages of RTD+HBT logic such as self-latching gates and single gate carry circuit implementation make them a potential candidate for ultrafast and ultradense VLSI circuit design. Along the same principles as RTD+HBT logic, RTDs have been used in conjunction with MODFETs to develop a new logic family. In the absence of enhancement-mode MODFETs, positive and negative supply voltages, and level shifting stages are used. Two-peak RTDs are used to obtain a large enough voltage separation between the peak and valley points, but either 1-peak or 3-peak RTDs could be used instead, with a corresponding change in the voltage margins. The circuit consists of two stages; the first stage is a 3-input bistable minority gate. The second stage is a combinational inverter that produces the majority function. The combinational inverter has a depletion MODFET load instead of an RTD load. The combinational inverter has a depletion MODFET load instead of an RTD load. When the input to the inverter is low, the driver transistor is turned off and the output is high. When the input to the inverter is high, the driver is turned on and the output is pulled low. The inverter is very similar to an inverter in buffered FET logic (BFL). The depletion-mode MODFETs have a threshold voltage of approximately -0.6 V. The supply voltages are 1.5 V and -2.0 V. The input and output logic levels are -0.2 V and -0.7 V. The RTDs have a peak voltage of approximately 0.1 V and a valley voltage of approximately 0.4 V. The peak and valley currents of a $1\mu m \times 1\mu m$ RTD are 100 μA and 25 μA, respectively. Two level shifting diodes are used. Basic RTD+MODFET bistable logic gates (NAND, NOR, MINORITY) have been fabricated in collaboration with Texas Instruments, Inc. Table 1 which shows the comparison of the device counts of NDR logic circuits with similar implementations in conventional technologies.

Table 1: Device Counts for Function Implementation in Various Technologies

Circuit	**TTL**	**CMOS**	**ECL**	**NDR**
Bistable XOR	33	16	11	4
Bistable Majority	36	18	29	5
Muller C-element	45	8	44	4
9-state memory	24	24	24	5
NOR2+flipflop	14	12	33	4
NAND2+flipflop	14	12	33	4

- **Theoretical analysis of NDR circuits:** A concern of RTD-based logic circuits is their reduced noise margin due to operation in the threshold mode. We have developed a noise margin measurement technique for RTD+HBT logic gates adapted from the simple but accurate method of fitting a maximum area rectangle between the normal and mirrored transfer characteristics of an RTD+HBT

inverter. This method is very general and precise for characterizing noise margins. Additionally, due to the nature of the transfer characteristic of an RTD+HBT inverter, this method can be applied very simply, with some modifications. Also, due to the presence of a clock line, noise margin calculations must account for noise on this line as well. The final equations for noise margin of RTD-HBT circuits are presented below.

$$NM_H = (V_{cc} - V_p) + (I_{clkh} - I_{clkq} - \delta_I)R_{p1} \quad - V_T ln\left(\frac{I_p - I_{clkh} + \delta_I}{I_s\left(1 - e^{-\frac{V_{cc}-V_p}{V_T}}\right)}\right), \quad (1)$$

$$NM_L = V_T ln\left(\frac{I_p - I_{clkh} - \delta_I}{I_s\left(1 - e^{-\frac{V_{cc}-V_p}{V_T}}\right)}\right) \quad - (V_{cc} - V_s) - (I_{clkh} - I_{clkq} + \delta_I)R_{p2}. \quad (2)$$

Also the RTD parameters provide a figure of merit for noise margin that can be written as below.

$$NM_H + NM_L < (R_{p2} + |R_n|)(I_p - I_v) \quad + (R_{p1} - R_{p2})(I_p - I_v) < V_v\left(1 - \frac{PVVR}{PVCR}\right). \quad (3)$$

Computer simulation of noise margins performed to compare experimental and theoretical results yielded good agreement. Since RTD+HBT circuits operate at extremely high speeds, it is imperative to account for the ΔI-noise generated by the sharp clock edges coupled with the inductances of interconnects. Also, it can be seen that the upper bound on the sum of the noise margins ($NM_H + NM_L$) that can be extracted from a given RTD, irrespective of the type of transistors used, can never exceed the valley voltage, V_v, of the RTD. To maintain consistent output high and low voltage levels in order to have reliable operation of cascaded gates, it is necessary to have small values of positive differential-resistances, R_{p1} and R_{p2}. This combined with the need to have high $PVCR$ and low $PVVR$, indicates that the ideal RTD characteristic would have a sharp 'N' shape. Along with noise margins, the theoretical analysis of speed and power dissipation of RTD-based circuits, shows that these circuits have considerable power-delay product advantages over conventional circuits. A summary of basic quantum circuit designs is presented in Table 2. The entries for power in Table 2 are for circuits operating at the maximum speed corresponding to the entry for speed/delay for that circuit.

- **Multi-valued logic and analog circuits:** A significant advantage of resonant-tunneling devices is the multistate nature of MRTDs which can provide compact and high-speed multivalued circuit alternatives for conventional binary circuits. Multiple-valued logic (MVL) has been shown to effectively reduce the number of interconnects in digital circuits. Interconnection length and complexity will be the

Table 2: Summary of Basic Self-latching NDR Circuits

Circuit	**Technology**	**Power (mW)**	**Speed/ Delay**	**Noise Margin**
AND3	RTBT	10	40 ps	0.3 V
OR3		10	37 ps	0.3 V
CARRY		10	34 ps	0.3 V
NOR3	RTD+	0.48	5 GHz	I_h=90 mA
MINORITY	MODFET	0.6		I_l=0
NAND3	(dep.)			NM_l=9 mA
				NM_h=17 mA
NOR3	RTD+	0.3	5 GHz	same as
MINORITY	MODFET			above
	(enh.)			
NOR3	RTD+HBT	0.5	25 GHz	0.3 V
MINORITY				
Adder		10	800 ps	
(32-bit)				
Correlator	RTD+HBT	320	10 GHz	
(32-bit)	RTD+	250	3 GHz	
	MODFET			
T-gate	RTD+HBT	327	2.87 ns	0.3 V
		3.2	33.3 ns	
MVL Gate		500	2 GHz	
Array				

dominant limiting factor of integrated circuit performance as device dimensions continue to shrink while chip areas continue to grow. The enhanced signal encoding efficiency of MVL results in a factor of $log_2 r$ reduction in number of wires for a radix-r number system as compared to an equivalent binary logic circuit. This in turn facilitates increased speed of operation and decreased power consumption in a logic circuit. We have developed a multiple-valued logic multiplexer that uses the RTD characteristic to pick specific ranges in the input voltage. Although this design uses RTD+resistor branches as in the previous gate, the RTD branches are all coupled so that when one switches on, the others switch off. When the input voltage to the RTD is in a specific narrow range, the HBT is turned on and the output voltage goes low. In the complete multiplexer circuit four such RTD selectors are coupled together through the use of resistors R_2, R_3, and R_4. The input voltage to each successive stage is a diminished version of the *select* input voltage, due to the voltage drop in the resistors R_2, R_3 and R_4. These resistors are chosen so that each HBT connected to the RTD branches turns on at different ranges of the input voltage. Further, when one RTD switches abruptly to the lower base voltage state, the current in the next RTD branch increases suddenly, causing the corresponding HBT to switch *on* immediately. The outputs of all the RTD branches are connected to current switches, whose *on* currents are proportional to the input voltages. The RTD branches ensure that all but one of the summed currents are 0 and the other summed current is proportional to the selected input voltage. By properly choosing the output resistance, the output voltage is made equal to the selected input voltage. The RTD multiplexer is thus a four-input analog multiplexer with a single multiple-valued select line. When the input signals are restricted to four different logic levels, the multiplexer becomes a four-valued T-gate. The T-gate is an extremely versatile building block for multiple-valued logic and any multiple-valued function can be implemented using T-gates alone (along with constants). The RTD+HBT multiplexer uses 4 RTDs, 21 HBTs and 16 resistors while a CMOS circuit with equivalent functionality (binary, 2-bit 4:1 multiplexer) would require 44 transistors (MOSFETs). The savings in area increase with higher-valued logics. For an 8-valued T-gate (8:1 multiplexer), the multiplexer design described above can be extended by using eight literal-pass gates with tighter margins on input voltages. Such a multiplexer would use 25 transistors and 32 resistors as against 118 MOSFETs for an equivalent CMOS implementation (binary, 3-bit 8:1 multiplexer).

We have designed a compact one and two-input multiple-valued logic gate which can be mask programmed or be synthesized following simple rules. The mask programmable design is ideal for use in gate arrays not only because its MVL input and output lines require less space to route than its binary counterparts, but also because of the fact that even the functionality of these gates can be changed at the last mask levels. This provides tremendous design flexibility while vastly reducing design turnaround times. The design can be implemented with fewer transistors

than other reported methods because of the use of RTDs. The decoder generates a logic high in one of its four outputs (L-lines) based on the input's logic level. It is made up of four literal circuits each turning on at a different non-overlapping voltage range. Literals can be implemented very efficiently using a vertical integrated structure of an RTD and an HBT that forms a resonant-tunneling bipolar transistor (RTBT). The literal circuit consists of an RTBT inverter whose output is connected to a normal inverter. The quantizer converts a logic high on one of its inputs (Q-nodes) to a predefined voltage level. Together, the gate can be mask-programmed by connecting each L-line to some Q-node. It is designed as a current mirror with multiple input resistors of different values. The fact that only one decoder output is high and all the others are reverse biased at any one time simplifies the design of the quantizer.

We have also designed a compact four-valued down counter using RTDs and HBTs. It uses three transistors and one four-peak RTD. An equivalent counter implemented in CMOS would require 30 transistors. Thus, considerable area and circuit component count reduction arise as a result of RTD-based implementation of MVL circuits.

- **System design using NDR devices:** The self-latching nature of basic NDR gates, and the ability to implement extremely compact MAJORITY gates in NDR logic leads to new possibilities for fast adder designs that utilize gate-level pipelining to provide very high addition throughput. Thus, a new system design technique, called nanopipelining, is made possible in which primitive logic gates also perform the latching function without the necessity for external latches. This eliminates delay and area overhead in pipelined systems, thus further improving speed and throughput of deeply pipelined systems over what can be gained as a result of the picosecond switching speeds of RTDs. A gate-level pipelined adder has been designed using RTTs, RTD+HBTs and RTD+MODFETs. In this circuit, two computations can be active concurrently and this is how nanopipelining improves the throughput of the system.

  A multibit adder is an essential part of any general purpose computer, and a trade-off is normally made between the speed and area of the adder, since fast adders usually require more hardware. A simple *ripple carry* adder requires the least number of gates, but the time required to perform a single addition is a linear function of the number of bits in the numbers being added. A *carry lookahead* adder requires more logic but its speed is, ideally, independent of the number of bits being added. However, practical considerations such as fan-in and fan-out limitations cause the carry lookahead scheme to be slower than in the ideal case. Variations on this theme, such as the Ling adder seek to overcome the fan-in limitations by using WIRE-OR properties of certain logic families along with some algebraic

manipulation of the terms in the carry-lookahead expressions. Another type of fast adder makes use of chains of pass gates (CMOS) to form the sum and carry, in effect replacing multiple gates with a single complex gate. However these adder architectures are technology specific, and cannot be used if the technology does not permit wire-or or the chaining together of a large number of transistors in series. The nanopipelining concept was used to design fast multi-bit adders using only a small number of cyclically connected bistable full adders. A 64-bit adder was chosen as the vehicle to explore the design problem. A four-bit adder formed the basic building block for the larger adder. Each adder has 4 stages corresponding to the 4 levels of the true-bistable sum circuit. The carry output is generated in the first stage, while the sum output is generated in the 4th stage. Since 2-phase clocking is used, the data at the input changes once every two time periods. The feedback scheme feeds the carry bit from the fourth adder back to the input of the first adder. Since the carry bit is delayed by four clocks, the bits a_4 can enter the adder only at time $t = 9$. To improve adder utilization four different additions can be interleaved. The interleaved serial-parallel data format allows four different additions to proceed simultaneously. A 64-bit addition has a latency of 63 time units but the throughput of the adder is increased to one 64-bit addition every 16 time units. A conventional serial-parallel ripple carry adder that performs 4-bit ripple carry addition on a series of 4-bit wide inputs, with the carry from the MSB being clocked and fed back, has a latency of 63 t_c, where t_c is the time required to generate the bit-wise carry (at least 3 gate delays for each bit) and a throughput of one 64-bit addition every 64 t_c time units. The nanopipelined NDR adder architecture improves the throughput to one 64-bit addition every 16 t_{cndr} units, where t_{cndr} is the bit-wise carry generation delay and is equal to one gate delay instead of three gate delays in conventional logic. Hence the nanopipelined architecture increases the throughput by a factor of 12 without any significant increase in area as compared to the conventional serial-parallel pipelined addition scheme. The number of gates required is about 30, compared to the 600 required for carry lookahead addition. The complete 64-bit pipelined adder uses four identical single-bit adders with the carry-out of each adder being connected to the carry-in of the next adder in a cyclic fashion. The 64 bit numbers are fed to this adder in a bit-serial fashion and four different additions are carried on simultaneously in the four pipeline stages. The effective throughput of the pipeline system is thus one new 64-bit addition for every 16 time units or one new 32-bit addition every 8 time units; with a clock period of 100 ps this gives an effective throughput of one 32-bit addition every 0.8 ns or one 64-bit addition every 1.6 ns. Since the entire adder contains only about 30 gates, with an area of 26μm $\times$ 36 μm per gate, the maximum interconnect length is around 300 μm. Using a capacitance factor of 4 fF/100 μm for GaAs, the total line capacitance is only 12 fF, or about a third of the input capacitance of a single HBT. Hence, the effect of interconnect delay is minimal in this design. The effect of line inductance for such line lengths is also negligible. Hence, we see that nanopipelining can improve the throughput of

multi-bit adders due to elimination of area and delay overhead of pipeline latches that are present in conventional designs. In particular, the speedup proffered by nanopipelining is highly evident in circuit systems that use long, cascaded adder trees.

We have designed a 32-bit parallel correlator, an important constituent block of a code division multiple access (CDMA) system, that exploits the system-level advantages of RTD-based nanopipelined adders. CDMA systems provide highly secure, reliable, and noise-free transmission between two transceivers. However, CDMA systems typically use very long pseudo noise (PN) sequences (> 1000 chips) and hence require a tremendous amount of bandwidth since each transmitted bit is encoded into as many chips as the PN code length. Thus, to achieve reasonable speed of transmission and reception, it is imperative that high performance circuits be used that maximize the symbol transmission rate. Quantum effect circuits can hence play a vital role in improving the speed of CDMA systems. High-throughput CDMA systems that use long PN sequences require very high-speed parallel correlators. We have designed an RTD+HBT based 32-bit correlator consisting of a nanopipelined adder network that has a simulated effective throughput of one 32-bit correlation every 100 ps. The correlator is an ideal vehicle for demonstrating the advantages of NDR logic since it utilizes long adder trees that can efficiently be implemented using nanopipelining logic of RTD-based circuits. A 32-bit latch holds the PN sequence. The input is a serial bit stream which is fed to a 32-bit shift register. The 32-bit latch and 32-bit shift register are each composed of 64 bistable RTD+HBT inverters. A pair of cascaded bistable inverters each operating on single, separate phases of the two-phase clock form the basic 1-bit latch. The 32-bit raw correlation vector is generated by performing a bitwise XOR operation on the PN sequence latch output and the most recent 32 bits of the sampled signal available at the shift register output. The raw correlation vector is automatically latched at the output of the XOR network due to the use of self-latching gates. This vector forms the input to the pipelined adder network that determines the difference between the number of 1s and 0s in the raw correlation vector. The result of this operation is the correlation value between the incoming signal and the resident PN sequence and is determined for the 32 most recent data bits at every clock cycle. This value ranges from -32 to $+32$. The adder network consists of 26 nanopipelined full adders, 11 nanopipelined half adders, and 36 bistable inverters. The adders used in the design have complemented sum and carry outputs in order to reduce pipeline latency. The input to the adder network is the raw correlation vector generated by the 32-bit bistable XOR network. The circuit performs eighteen stages of addition to generate a 7-bit result which is the difference between the number of 1s and number of 0s in the correlation vector. Since each stage is nanopipelined, the throughput of the circuit is one 32-bit correlation every cycle. However, since the seven bits of the adder network output are not simultaneously generated, bistable inverters are required to synchronize the bits such that all seven bits of a correlation appear in

order at the output of the correlator. The least significant bit of the correlation value is always 0 since the difference between the number of 1s and number of 0s in a 32-bit vector is always even. The pipelined adder network essentially sums up the number of 1s in the correlation vector. Bits 0, 1, 2, 3 and 4 of the sum of 1s directly translate to bits 1, 2, 3, 4 and 5 of the difference between number of 1s and number of 0s. Bit 6 of the correlation value is computed while bit 5 of the sum of 1s is being generated by connecting the carry input of the final full adder to V_{cc}. This achieves the 2s complement subtraction required for computing the difference between the number of 1s and number of 0s in the correlation vector. No additional pipeline stages are required for this conversion.

- **CAD tool development for NDR devices and circuits:** In the device design stage, a device simulator which solves the Schrödinger and Poisson equations self-consistently, including phonon scattering effects, is used to obtain the most desirable I-V characteristics for the device. The resulting I-V characteristics are then used in a circuit simulator to simulate quantum circuits. We have developed a quantum circuit simulator called NDR-SPICE, incorporating device specific convergence routines, which can overcome many of the convergence problems that SPICE-like circuit simulators face while dealing with negative differential resistance devices. This simulator has enabled us to simulate many previously hard-to-simulate quantum circuits.

  At high frequencies of operation, the interconnects play a crucial role in determining circuit performance. It is not always possible to incorporate the interconnect delays right at the time of circuit simulation, since the layout and processing information are not readily available at that stage and as such, the simulation results are always too optimistic. We have developed a simple Delay Estimator tool which is capable of projecting a more realistic circuit performance than that offered by circuit simulators alone. From the SPICE description of a circuit, the Delay Estimator determines the number of terminals that need to be connected. By using Rent's rule, it estimates the interconnect length distribution in the circuit and represents these interconnects by means of various models. The resulting augmented circuit is then simulated to obtain a realistic picture of the performance of the circuit.

  We have proposed an optimization technique for RTD-based circuits that maximizes design tolerances and minimizes power dissipation, based on a modified simplex method. The optimization scheme is well applicable to all self-latching circuits and also to multiple-state memory design. The key features of the optimization technique are: a) Switching conditions are described by linear in-equations in the line currents and the RTD peak/valley currents; b) A graph-based technique is used to derive the relationships between all the constraints and extract a minimal set of non-redundant constraints; c) Objective functions can either be a continuous

function of the currents such as power consumption, or a min-max function on the margins. Since these objective functions are not all linear in the input variables, non-linear optimization techniques must be used. In particular, a methodical search in margin space using Multiple Linear Programming approach, has been successful in initial attempts at solving this problem.

SIGNIFICANT RESULTS:

- Device and Circuit Fabrication
  - InP-based RTBT is fabricated with a cut-off frequency (f_T) of 77 GHz and a maximum oscillation frequency (f_{max}) of 60 GHz.
  - GaAs-based RTBT devices are processed with a f_T and f_{max} of around 30 GHz.
  - InP- and GaAs-based HBT devices have been developed with better performance than RTBT devices.
  - Fabrication of bistable mode low-power monolithic IC's, which were implemented using HBT and RTD for realizing compact digital functions, namely, NAND, inverted majority gate, bistable NOR, etc.
- Circuit Design and Analysis
  - Development of a RTD-HBT bistable mode logic family.
  - Development of a RTD-HEMT bistable mode logic family.
  - Theoretical analysis of RTD circuit topologies for accurate projection of noise margin, switching speed and power dissipation.
  - Design and test of basic multiple-valued logic circuits such as literals and T-gates using RHETs or RTBTs or a combination of RTDs and HBTs.
  - Design and implementation of an RTBT and RTD-HBT multivalued multiplexer and analog channel selector. HBTs.
  - Design and test of a compact ADC circuit using multipeak RTDs.
  - Design of a four-valued down counter using RTDs and HBTs.
- System Design
  - Development of a new system design technique called nanopipelining that allows pipelining at the gate level with no area/delay overhead of pipeline latches.
  - Design of a highly pipelined 64-bit adder using RTTs.
  - Design of a 32-bit parallel correlator using RTD+HBT and RTD+HEMT logic.

- Circuit Simulation and Optimization
  - Developed a new flexible and accurate circuit simulator for NDR devices.
  - Added variety of simulation models for RTDs, RTTs, MPRTDs, and STTs to the NDR simulator.
  - Studied convergence problems of NDR device simulation in conventional simulators and developed new algorithms to alleviate these problems in our NDR simulator.
  - Developed a statistical optimization tool in order to meet multiple conflicting constraints in NDR circuit design.
  - Developed an interconnect delay estimator for realistic performance projection of NDR circuits and systems.

PUBLICATIONS:

No new publications since last report, January, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

INTERACTION WITH OTHER D.O.D. LABORATORIES, INDUSTRIES AND UNIVERSITIES:

- Hughes Research Laboratory: Fabrication of RTD+HBT logic circuits and parallel correlator.
- Lockheed-Martin Inc.: Fabrication of RTD+HBT multivalued logic circuits.
- Texas Instruments Inc.: Fabrication of RTD+HEMT logic circuits and bistable full adder circuit.
- Mayo Clinic: Testing of high-speed RTD-based circuits.
- Naval Research Laboratory: Material growth for RTD circuits.

VII. LASER SOURCES BASED ON INTERSUBBAND TRANSITIONS

FACULTY SUPERVISORS: G. I. Haddad
T. Norris

RESEARCH SCIENTISTS: X. Zhang
J. P. Sun

GRADUATE STUDENT PARTICIPANT C. Y. Sung
A. Afzali-Kushaa
H. B. Teng

PERIOD: July 1, 1992 -June 30, 1998

TASK OBJECTIVES:

The objectives were to investigate the potential of using intersubband transitions in quantum wells and strained layers for various devices including detectors, modulators, and sources. The advantages of using quantum wells lie in that the emission wavelength can be tailored from the mid-infrared to terahertz frequency range, and that the choice of the material system is not limited to direct band gap materials. These advantages open the possibilities of extending the devices to longer wavelengths and utilizing a greater variety of materials for these devices.

WORK PERFORMED:

1. MBE growth was performed for samples of step quantum well laser structures; FTIR spectrometer measurements were performed for intersubband absorption spectrum; photoluminescence measurements were carried out to observe optically pumped interband emission; time resolved femtosecond differential transmission spectroscopy measurements were performed to observe population inversion.

2. Computer programs for calculations of electron and hole wavefunctions, subband structures, intersubband relaxation rates, and population inversion in step quantum well structures were developed. Computer programs to calculate the localized phonon modes, electron relaxation rates based on these phonon modes in the quantum well structures were also developed.

3. Design simulations were performed using the computer programs developed for realistic device development in the research project.

4. Approximately 17 conference presentations and research papers related to the laser sources work were presented or published during this period.

MAJOR ACCOMPLISHMENTS:

1. Several schemes using either electron or hole intersubband transitions for laser sources in the far infrared and terahertz frequency ranges were conceived and studied. Both quantum well and strained systems were investigated.

2. We proposed and investigated a new electrically pumped intersubband laser at 10 μm wavelength, in which population inversion was demonstrated between subbands in an asymmetrical step quantum well structure.

3. We have also observed population inversion between subbands separated by 7 THz in step quantum wells designed for an optically pumped intersubband laser.

4. A tensile strained THz-laser based on a p-InGaAs/InP heterostructure was investigated experimentally and strong absorption between the LH- and HH-valence bands was observed and studied.

5. The electron relaxation times between the subbands were investigated both theoretically with quantum models and experimentally using time resolved femtosecond measurements. Consistent results between the calculations and experiments were obtained.

6. Theoretical studies were performed for evaluation of effects of localized phonons on the electron relaxation rates between the subbands in various quantum well structures designed for intersubband lasers, which will be very useful for design optimization of intersubband laser structures.

PUBLICATIONS:

1. SeGi Yu, K. W. Kim, M. A. Stroscio, G. J. Iafrate, J. P. Sun and G. I. Haddad, "Transfer Matrix Method for Interface Optical-phonon Modes in Multiple-interface Heterostructure Systems," *J. Appl. Phys.*, **82**, 3363-3367, 1997.

2. J. P. Sun, H. B. Teng, G. I. Haddad, M. A. Stroscio and G. J. Iafrate, "Intersubband Relaxation in Step Quantum Well Structures," The Fifth International Workshop on Computational Electronics, Notre Dame, Indiana, May 28-30, 1997; also to appear in *VLSI Design*, 1998.

3. J. P. Sun, H. B. Teng, G. I. Haddad and M. A. Stroscio, "Electron-interface Phonon Interaction in Multiple Quantum Well Structures," The Second International Workshop on Surfaces and Interfaces of Mesoscopic Devices, Maui, Hawaii, Dec. 7-12, 1997; also to appear in *Semiconductor Science and Technology*, 1998.

Ph.D. STUDENTS GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since the last report, January, 1998.

INTERACTION WITH ARMY LABORATORIES:

Close collaboration and many technical discussions with Dr. Michael Stroscio of Army Research Office on localized phonon theories and quantum laser designs.

VIII. DESIGN, FABRICATION AND CHARACTERIZATION STUDIES OF HETEROJUNCTION BIPOLAR TRANSISTORS

FACULTY SUPERVISOR: D. Pavlidis

GRADUATE STUDENT PARTICIPANTS:

D. Cui
D. Sawdai
J. W. Park

PERIOD: July 1, 1992 – June 30, 1998

TASK OBJECTIVES:

The properties of heterojunctions grown by Metalorganic Chemical Vapor Deposition (MOCVD) were investigated as applied to high-frequency heterojunction electronic device application. The use of carbon as dopant in Heterojunction Bipolar Transistors (HBTs) was explored and the carrier lifetime of C-doped layers was studied. GaInP/ and InP/InGaAs HBTs were designed, fabricated and characterized and integrated circuits using such devices were studied.

MAJOR ACCOMPLISHMENTS:

A new formulation has been developed that allows analytic calculation of the frequency dependent current gain and power gain roll-off in HBTs, along with new and accurate expressions for f_T and f_{max} that take into account coupling between various charging times, coupling between charging and transit times, and the effects of parasitic elements such as inductances and other series access components. The technique is based on the HBT T-Model small-signal equivalent circuit and the analytic extraction of that equivalent circuit directly from the S- parameters. This approach provides clear insight into the causes of deviation from single pole 20 dB/decade roll-off in $|h_{21}|^2$ as a function of frequency.

Velocity overshoot effects have been studied in the pre-collector region of Heterojunction Bipolar Transistors (HBTs). Analytic expressions for the HBT pre-collector transit delay time, τ_{PCD}, have been derived and thoroughly investigated as a function of peak velocity (v_p) and mean free time to the peak velocity (τ_p). It is found that for a given peak velocity, minimum delay times are achieved when the velocity peak occurs at the midpoint of the pre-collector thickness. A three valley Monte Carlo simulation was used to generate velocity profiles as a function of time, and the proposed

analytic two-region model was matched to these v(t) profiles for different electric field conditions with excellent correspondence. This approach allows the accuracy of Monte Carlo techniques to be applied analytically without the need for the implementation of a Monte Carlo simulation code that takes a long time to develop and run. The Monte Carlo results are then used as a physical basis for the analytic description of velocity overshoot effects in actual GaAs pre- collectors as a function of electric field, allowing for the first time direct analytic calculation of pre-collector transit delay taking overshoot effects and electric field dependencies into account.

Novel approaches to the calculation of small-signal current gain and power gain of HBTs have been developed and implemented. Based on the T-Model equivalent circuit, these analytic expressions result in highly accurate analytic expressions for f_T and f_{max} that are compared with conventional equations based on the hybrid-pi equivalent circuit topology. Extrapolation techniques used to estimate f_T and f_{max} are evaluated and are found to often underestimate the actual intercept frequency, with an experimental example presented here demonstrating a 50% error in f_T using extrapolation. A criteria for accurate use of extrapolation is described for both f_T and f_{max}.

The low frequency noise characteristics of self-aligned, power GaAs/AlGaAs HBTs have been measured. The results here are especially important since the category of device tested will invariably be used in non-linear applications where up-conversion of low frequency noise would be inevitable. Selection of an appropriate two port noise model was outlined. It was determined that the most representative two port noise model for a noisy HBT was the short circuit noise current model. A measurement procedure for this type of model was described. It included corrections for the system noise floor and finite device input impedances. The measurements spanned 10 Hz to 100 kHz for a wide range of bias conditions. In all cases a $1/f^{\gamma}$ component was found for f<100 Hz. The value of γ was bias dependent. This is either not observed or discussed in other work on GaAs/AlGaAs HBTs. Large deviations from $1/f^{\gamma}$ at higher frequencies were caused by trapping. Variations in the magnitude of the noise, among the devices, was large; at a fixed collector current density the collector noise was found to vary by as much as 10 dB at 10 Hz. The bias dependence of the base noise spectra and the collector noise spectra indicated that recombination was the mechanism responsible for the 1/f type of noise. The absence of diffusion 1/f noise clearly indicates that the noise of these devices was not at the fundamental limit, hence further improvements can be made. The noise spectra did not display significant V_{CE} dependence at low collector currents, however, changes in the spectra could be observed at higher collector currents. Temperature dependent measurements determined that the most prominent trap had an activation energy of about 0.58eV.

A simplified intrinsic noise model was developed to help understand the low frequency noise properties of HBTs by using circuit topology dependent spectral measurements. With emitter feedback, $S_{IC}(f)$ decreased significantly while $S_{IB}(f)$ decreased much less.

In contrast, the spectra of Si BJTs show little change. It was demonstrated that the terminal noise was due to at least two intrinsic noise sources. For low bias conditions, the terminal noise could only be approximated by one source in the base-emitter region dominating $S_{IB}(f)$, and one source between the collector and the emitter dominating $S_{IC}(f)$. A more complicated intrinsic noise source model than the one used here is needed to model the noise more accurately.

In the area of large-signal modeling we analyzed both AlGaAs(GaAs) and InP/InGaAs HBTs as incorporating thermal effects in a self-consistent way and developing models that could be incorporated in commercially available players, such as Libra/ESSOF.

A breakdown model has been developed and incorporated in the large signal modeling of InP-based HBTs and accounts for their "soft-breakdown characteristics.

A Gummel-Poon large-signal model incorporating self-heating effects was employed for the analysis of the microwave power characteristics of HBTs. The model has been implemented in a commercial microwave circuit simulator. The impact of self-heating effects and bias on HBT large-signal performance was studied. RF excitation was found to reduce self-heating effects on devices biased with a constant I_B. On the other hand, constant V_{BE} bias enhances the ability of HBTs to deliver maximum output power. The HBT thermal capacitance, C_{th}, was found to be beneficial for large output power operation when constant I_B is used but does not play a significant role in the case where constant V_{BE} bias is employed. Constant V_{BE} bias is more suitable for high power HBT applications.

Heterojunction Bipolar Transistors (HBTs) are widely accepted as the most promising devices for power applications. MMIC design using such devices requires precise characterization and e valuation of the intermodulation (IMD3). The latter characteristics are commonly obtained by manual evaluation of the devices which does not allow precise knowledge of device-level characteristics and misses very often critical regions of operation where performance can be optimized or tradeoffs can be made. To overcome these limitations. We made use of a fully automated on-wafer source/load pull measurement with specially developed for this purpose software which allows complete mapping of the impedance plane of a Smith Chart in terms of P_{out}, PAE and IMD3.

InP/InGaAs HBTs were grown by our in-house MOCVD system and devices were fabricated using self-aligned technology. A systematic investigation of single HBT designs based on InP was carried out in order to evaluate their suitability for power applications. A study of this type is important due to the absence of heterojunction spike at the base-collector (B-C) interface of SHBTs and thus excellent high frequency performance compared for example to DHBTs which are traditionally the preferred candidates for power applications.

The DC, small-signal, and power characteristics were studied as a function of device geometry. Devices with variable emitter-finger size (2x10, 2x20, and 3x10μm^2) and number of fingers (1, 2, 4 and 10) were analyzed. Considering the single heterojunction design, these devices offered a high output power level of 2.74 W/mm for a 4-finger (2x10μm^2 each) HBT and a high power-added efficiency (PAE) of 43% for a 4-finger (2x20μm^2 each) HBT at 10 GHz, both biased by constant V_{be} under class A operation with optimally-matched source and load impedance.

Self-aligned composite and traditional GaInP emitter designs were fabricated using Chemical Beam Epitaxy (CBE) layers with TBA/TBP precursors. The C_{BE} of composite emitter HBT was found to be significant lower than that of traditional designs and presents a weak J_c dependence. This feature leads to enhanced f_T performance for the new HBT designs. Best microwave performance for composite emitter HBTs was f_T = 60 GHz and f_{max} = 75 GHz for a 2μmx30μm emitter device.

To investigate the possibility of using C instead of Zn in InP-based HBTs, C- doped InGaAs layers were grown and characterized by Fourier Transform Infrared Spectroscopy (CFTIR). C-doped InGaAs was grown by MOCVD on InP (100) substrates using a CBr_4 source and doping levels of 3x10^{19} cm^{-3} have been achieved. The presence of an aligned [H- $(C_{AS})_2$] complex is evidenced at the growth surface of C-In_x $Ga_{1-x}As$ layers for x=0.53 by FTIR measurements. Further evidence of passivation mechanism taking place by hydrogen incorporation in the layer is expected by performing liquid Helium temperature IR measurements, with higher resolution, in order to resolve the observed peak.

To optimize the characterization of InGaAs/InAlAs heterojunctions as necessary for high frequency device applications, InGaAs single quantum wells in InAlAs barriers have been grown by MOCVD with different growth interruption times at the well interfaces. Low temperature PL showed the existence of a 2D electron gas in the well, and allowed the estimation of gas density in agreement with Hall measurements. A large growth interruption time (15s) introduces non-radiative impurities at well interfaces. Despite the high residual doping level of the layers, room temperature PR measurements were performed, and showed that the broadening parameter of quantum confined transitions varies quadratically with quantum index n. Growth interruption times up to 15s were shown to reduce interface roughness. The results are in good agreement with an increase of Hall mobilities as the growth interruption time is increased.

WORK PERFORMED:

The heterointerface properties of InGaAs/InAlAs HEMTs have been studied by photoreflectance. InGaAs/InAlAs quantum wells (QWs) have been grown for the purpose of MOCVD. A one-dimensional, one-particle, Schrodinger-like wave equation obtained from an envelope function approximation was solved numerically to determine the subband

of this structure. The results obtained from this study show that increasing the growth interruption time from 0 to 15 s increases the abruptness of the well barrier interfaces and results in an increase of the carrier mobility of the corresponding two-dimensional electron gas. The resulting change in shape at the top of the QW leaves the ground state transition energies unchanged, while the higher order transition energies are modified. This, in effect, results in a change of the optical properties while maintaining the same band-gap of the QW structure. In addition, the PR results show how this technique can be used simply as an effective characterization tool to evaluate the quality of the QW heterointerfaces as determined by the QW transitions.

While rectangular QWs are desirable for the in depth understanding of the material and devices, nonideal structures with graded interfaces may in fact be preferable for devices as the less abrupt interfaces enables fast carrier removal for high speed switching.

GaInP/GaAs HBTs were studied as discrete, as well as, integrated components using Chemical-Beam-Epitaxy (CBE) grown materials. Alternative group V sources tertiary-butylarsine, tertiarybutylphosphine, and trisdimethylaminoarsenic are used instead of traditionally employed AsH_3 and PH_3. A very high degree of reproducibility of growth parameters (fluxes, substrate temperature, doping levels) is demonstrated. Total defect densities lower than 10 def/cm^2 are routinely obtained. Large-area GaInP/GaAs heterojunction bipolar transistors (HBTs) show a high current gain of 225 for base sheet resistance of 400 ohm/sq. The devices also exhibit excellent high-frequency characteristics. With current- gain cutoff frequency (f_T) of 60 GHz and maximum oscillation frequently (f_{max}) of 100 GHz monolithic integrated broadband transimpedance amplifiers using the above technology demonstrated excellent performance with a maximum bandwidth of 19 GHz and an associated transimpedance gain of 47 dBΩ.

PUBLICATIONS:

1. W. C. H. Choy, P. J. Hughes, B. L. Weis, E. H. Li, K. Hong and D. Pavlidis, "The Effect of Growth Interruption on the Properties of InGaAs/InAlAs Quantum Well Structures," *Appl. Phys. Lett.*, **72**, 338-340, 1998.

2. D. Pavlidis, "Metalorganic Chemical Vapor Deposition (MOCVD) Material Growth and Application to InP-Based Electronic Devices," *Proceedings of the IEEE International Conference on Indium Phosphide and Related Materials*, (IEEE-IPRM 98), Tsukuba, Japan, pp. 477-480, May 11-15, 1998.

3. J. Park, S. Mohammadi and D. Pavlidis, "GaInP/GaAs HBT Technology Using TBA, TBP Precursors and Application to Optoelectronic Circuits," presented at the 22nd Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE 98), Zeuthen, Germany, pp. 33-34, May 24-27, 1998.

4. J. Ch. Garcia, C. Dua, S. Mohammadi, J. W. Park and D. Pavlidis, "Growth Characteristics of Hydride-Free Chemical Beam Epitaxy and Application to

GaInP/GaAs Heterojunction Bipolar Transistors," *J. Elect. Mat.*, **27**, 442-445, 1998.

5. J. W. Park, S. Mohammadi, D. Pavlidis, C. Dua and J. C. Garcia, "GaInP/GaAs HBT Broadband Monolithic Transimpedance Amplifiers and Their High Frequency Small and Large Signal Characteristics," *IEEE MTT-S International Microwave Symposium Digest*, (IEEE Radio Frequency Integrated Circuits, RFIC 98), Baltimore, MD, **1**. 39-42, June 7-9, 1998.

6. C. Bru-Chevallier, Y. Baltagi, G. Guillot, K. Hong and D. Pavlidis, "Application of Photoreflectance Spectroscopy to the Study of Interface Roughness in InGaAs/InAlAs Heterointerfaces," *J. Appl. Phys.*, to appear, October 15, 1998.

INTERACTIONS WITH OTHER D.O.D. LABORATORIES, INDUSTRIES AND UNIVERSITIES:

Rockwell	Thomson-CSF
Northrop Grumman	Focus
TRW	

IX. InP-BASED DEVICES AND MONOLITHIC INTEGRATED CIRCUITS

FACULTY SUPERVISOR: D. Pavlidis

GRADUATE STUDENT PARTICIPANTS:

D. Cui
P. Marsh

PERIOD: July 1, 1992 – June 30, 1998

TASK OBJECTIVES:

InP-based devices were studied for high-frequency applications. Examples include High-Electron Mobility Transistors (HEMTs), Heterojunction Bipolar Transistors (HBTs) and two-terminal devices for signal mixing and multiplication. Emphasis was placed on discrete and monolithic integrated circuit performance optimization with such devices.

MAJOR ACCOMPLISHMENTS:

The noise measurement techniques applicable to on-wafer probing have been studied and compared experimentally and via the use of Monte Carlo simulations. The techniques were studied to determine their sensitivity to various tuner errors. The conventional technique based on the Y-factor technique showed greater sensitivity to error than the system based on cold noise power measurements. The latter technique demonstrated less uncertainly.

The microwave drain noise characteristics have been studied for conventional long (1.0 μm and 0.4μm) gate GaAs MSFETs and short ($\approx$0.15μm) strained InGaAs/InAlAs/InP MODFET. The total drain noise of the MODFET was found to be greater than the MESFETs over the entire bias range tested. This contradicts the F_{min} results where the MODFETs had very low noise in comparison; $F_{min} \approx 0.48$ dB at 10 GHz for MODFETs and $F_{min} = 1.5$dB at 10 GHz for MESFETs. Estimated relative parasitic contributions were found to be far greater for the MODFET noise than the MESFET noise. This is most likely due to the far greater g_m of the MODFET. The estimated intrinsic channel noise was greater for the MODFET structure as well.

In the area of microwave-monolithic integrated circuits, it has been shown that conversion gain is possible using InP-based InAlAs/InGaAs HEMT MMIC technology at 94 GHz. A simple large-signal analysis method based on harmonic content studies

is developed and applied to HEMT mixers, providing physical insight to the mixing mechanisms and explaining the relationship between the conversion gain and device parameters. High frequency design criteria are established by defining the first harmonic transconductance cut-off frequency ($f_{T,gm}$). HEMTs with different characteristics were used in the mixer realization and the experimental results are compared, yielding the design performance expected from device parameter considerations. Measured power and frequency characteristics of conversion gain also show the expected performance with the best conversion gain of 0.9 dB at the RF frequency of 94 GHz and with an LO drive of 2 dBm. The conversion gain variation is with ± 1 dB over the passband of the mixer.

The first monolithic fundamental FET oscillator at D-band has been demonstrated using our submicron pseudomorphic DH-InAlAs/InGaAs HEMT technology. The circuit design was based on accurate HEMT modeling based on multi-bias S-parameter characterization. The circuit uses dual feedback topology for enhanced negative resistances at D-band. The monolithic chip contained on-chip bias circuitry and an integrated E-field probe for direct signal radiation into a waveguide. The circuit oscillated at 130.7 GHz with an output power of -7.9 dBm at the drain voltage of 1.3 V using 90 μm gate periphery HEMTs. This is the highest fundamental frequency signal generation reported out of monolithic chips using three-terminal devices and demonstrates that InP-based HEMT MIMICs are promising candidates for monolithic signal source above 100 GHz.

Single-gate InAlAs/InGaAs HEMT mixers have been demonstrated at W- band using both hybrid and monolithic approaches with conversion gains of 1-2 dB. However, single-gate mixers require an external waveguide coupler for the combination of LO and RF signals, which defeats the purpose of fully monolithic integration. This can be solved by employing a dual-gate HEMT in the mixer design. Due to the electrical isolation of the two gates caused by the small capacitance between them, the RF and LO signal can be combined at the device level with good RF-to-LO isolation. Dual-gate FET mixers have so far been demonstrated at microwave frequencies for applications such as front-ends for direct broadcasting satellite (DBS) systems and have shown good conversion gain and moderate noise characteristics. The work carried out at Michigan is the first such demonstration using dual gate HEMTs in monolithic form at W-band. Dual-gate HEMT mixers were also developed and demonstrated excellent performance at W-band. This approach advances the art of millimeter- wave mixing by avoiding external LO-RF coupling and providing this on the chip.

Systematic studies have been performed on MOCVD growth of InP-based High-Electron-Mobility Transistors (HEMTs). This technique provides the possibility of introducing phosphorous containing layers in the HEMT structure and has attractive features regarding eventual production application of them. The growth was carried out in a vertical mass transport reactor with rotating susceptor. All-methyl metal organic sources were used for group V. Studies of the impact of growth temperature on

material characteristics showed the expected trends of reduced Hall background doping and increased mobility with reduced temperature for InGaAs and InP. InAlAs showed marginal dependence of Hall background on temperature. On the other hand this material showed minimum discrepancy between Hall and C-V data and best photoluminescence at higher temperatures. Complementary DLTS and SIMS studies performed on the same wafers suggested that 650°C is the best choice for InAlAs growth with minimum trap concentrations. Since this material is of high importance in the HEMTs, a compromise was made in InGaAs, InP characteristics and this temperature was chosen for all subsequent experiments.

In the area of InAlas/InGaAs HEMTs we have explored the possibility of further enhancing the performance of DH-HEMTs by employing a sub- 0.1μm Γ gate self-aligned process. A gate length of 0.07μm was achieved in this way and a maximum frequency of oscillation (f_{max}) of 350 GHz and a current gain cut-off frequency (f_T) of 180 GHz were obtained along with the full channel current of 1.2 A/mm. Theoretical simulation using 2-D ensemble Monte Carlo simulation has also been performed to optimize the DH layer structure and to study the transport characteristics of DH-HEMTs compared with their SH counterparts. DH-HEMTs showed larger transit time due to the interface roughness scattering at bottom heterointerface and real space transfer.

Quasi-1D channel InAlAs/InGaAs HEMTs have been implemented with shallow gratings to solve the gate leakage problem while preserving the advantages offered by the quasi-1D approach. Various channel widths have been realized to study the impact of the channel width on the DC and microwave performance. Due to the enhanced charge control in the quasi- 1D HEMTs, enhanced transconductance/source-drain current (G_m/I_{ds}) and transconductance/output conductance (G_m/G_{ds}) were observed. Compared with conventional HEMTs, the quasi-1D HEMTs showed degraded f_T due to additional parasitic capacitances and improved f_{max} due to better carrier confinement.

The intrinsic delay time of submicron InP-based HEMTs has been evaluated by coupling the delay time analysis with a 2-D Ensemble Monte Carlo simulation. The relationship between the delay time and the transit time is explained. It is shown that the delay time can be quite different from the transit time depending on the velocity modulation. The delay from each region of the HEMT is calculated. The delay from the gate region was the major contributor to the overall delay while that from the drain region was also important. The bias dependence of the delay in each region of the device was calculated to explain the bias dependence of the total.

PIN diodes are key elements for microwave switching and optical signal detection. Most results reported today refer to microwave PIN switches fabricated on GaAs and optical PIN detectors using InP-based materials. The use of InP-based PINs for microwave applications has drawn less attention, but offers unique and very attractive features, namely low insertion loss, due to the high mobility of InGaAs layers, reduced ohmic

contact resistance on such materials, and low turn-on voltage, as necessary for limiting applications of low-power InP-based electronics. Moreover, InP-based PIN diodes can be used for switching functions and are compatible with InP HBT and HEMT millimeter wave technology. We addressed these features by evaluating the discrete characteristics of InP- based PIN diodes and examining their use as microwave monolithic integrated circuit switches.

Schottky diodes offer good room-temperature noise performance for millimeter and submillimeter wave receivers. Traditional receivers use whisker-contacted Schottkys. However, whisker contact fabrication and assembly is expensive and the mechanical properties of the contact make them difficult to qualify for high-reliability applications such as space-based radiometers and radio telescopes. Planar structures offer superior mechanical stability and much lower assembly costs since the anode is contacted via an integrated metal bridge. As demonstrated here, the planar approach also allows integration of other receiver elements with the mixer diodes. Such integration is essential to further reduce fabrication costs to make millimeter receivers available for commercial applications. The characteristics of InP-based varactors have also been addressed by the authors elsewhere. The work under this project concentrates on InP-based mixers designs and their integration with antennae.

Integrated InP-based InGaAs diodes should benefit from InGaAs higher electron mobility (μ_e) relative to GaAs. InGaAs low ϕ_b~0.25eV relative to GaAs ϕ_b~0.9eV can reduce LO power (P_{LO}) requirements to 1/5th to 1/10th that of GaAs. Furthermore, this integrated approach could utilize the superior noise and gain properties of InP-based HEMTs and HBTs as IF/RF amplifiers and LO drivers. The quasi-optical approach, discussed here, uses a silicon substrate lens to eliminate substrate modes and provide high directivity of the radiation pattern. This approach eliminates the need for expensive machined waveguide components and assembly. Additional cost reductions could be obtained by using cast alumina lenses.

Experimental results obtained up to 180 GHz from such mixer diodes validated the approach and demonstrated excellent performance. For example, an InGaAs-based subharmonic mixer showed a single-sideband conversion loss of 10.5dB and double-side band noise temperature of 1164K at a very low LO power level of 1.1mW. The performed work demonstrated the feasibility of integrating mixer diodes with antenna and other interconnect metal structures on InP. Simulations indicate the potential for performance improvements with L_c decreasing to 9.6dB and T_{mix} decreasing to approximately 700K for anode sizes of 1 μm. A significant advantage of the InGaAs subharmonic mixers is that their P_{LO} requirements are approximately a factor of 02 to 0.37 of that required by GaAs technology. Another advantage of InGaAs mixer technology is that high-performance three-terminal device technology, available on InP, could potentially be used to integrate LNA front ends and IF amplifiers with the mixers, to form high-performance monolithic millimeter-wave receivers.

InP-based micromachined circuit approaches were explored. InGaAs/InP IR sensors were evaluated for this purpose. In order to permit technology studies using a well defined circuit approach. The layers were grown by MOCVD and the new micromachined IR sensor approach demonstrated excellent responsivity and detectivity characteristics, as well as integration compatibility with electronic devices for signal information and treatment. The new sensor offers simplicity in fabrication and good process control. It demonstrated a vacuum relative detectivity of 7.1 x 10^8 cm $Hz^{-1/2}/W$. This device shows already performance exceeding the best obtained characteristics of GAs/AlGaAs thermoelectric IR sensors. Compared with GaAs-based technology the InP-based sensor requires only seven mask steps and no back side process.

The presented results demonstrate the high potential of the InGaAs/InP sensor for thermoelectric infrared applications. Further improvement of its characteristics could be envisaged by evaluating the thermoelectrical thin film properties of InGaAs experimentally and further optimizing the IR sensor design. Applications of the sensor are not only limited to infrared detection and imaging but can for example, be envisaged for novel detection schemes such as monolithic detection of microwave power in InP microwave monolithic integrated circuits and application to circuit analysis and operation control. An extension of this technology is considered for use in millimeter-wave InP-based integrated circuits.

WORK PERFORMED:

Mixer diodes made on InGaAs were studied in terms of the technology used for their fabrication and the resulting noise properties.

The choice of plated versus evaporated Pt Schottky anode formation technology is shown to have a significant impact on junction quality and the noise temperature of InGaAs mixer diodes. The investigated diode layers were grown in-house via Metalorganic Vapor Phase Epitaxy (MOVPE) on an S.I. InP wafer. For anode diameters at and below 2 μm, plated anodes clearly show superior fabrication ($\sim$80%) yields relative to evaporated (below $\sim$5%). DC and low-/high-frequency noise characteristics were compared, as functions of dc current drive, for plated versus evaporated InGaAs Schottky contacts at 10 Hz-100 KHz and 1.4 GHz for 4- and 6- μm anode diameters. Plated anodes show distinctly lower ideality factors of $\sim$1.2 versus $\sim$1.4-1.66 for evaporated anodes. Plated Schottky contacts showed 5.5 dB lower noise levels in the range of 10 Hz-100 KHz and a lower noise temperature (220 K versus 360 K) at 1.4 GHz. Overall, relative to conventional evaporated Pt, plated Pt anode technology offers superior fabrication yield and should lead to higher receiver sensitivity especially when low IF frequencies are used.

An on-wafer large-signal computer-controlled measurement system using a high-precision electromechanical tuner has been developed at W-band. The system allows load-pull

and power saturation characterization of millimeter-wave devices, as necessary for the development of power amplifiers and other components for W-band applications.

The system was employed to characterize InP-based HEMTs. The results obtained from the latter studies, although related to non-optimized for this frequency devices, permit system validation by evaluation of constant gain and power contours at 77 GHz. A power gain of 5.5 dB was found at 77 GHz at P_{IN}=-25dBm for optimal impedance (28.6-j24.1Ω). When the output power was increased to P_{IN}=-7dBm, the gain was compressed to 4.5dB and the optimal impedance moved to (39.9- j43.5Ω). PAE at 102GHz was ~1% for P_{IN}=+3dBm. A value of 2.5% was recorded at 77 GHz which appeared to increase for power levels close and above P_{IN}=-7dBm.

Use of the W-band on-wafer load-pull system was also made for evaluating the power-handling capability of W-band InGaAs PIN diode switches. It was found that InGaAs PIN switches did not demonstrate any degradation of Pout (Pin) characteristics for input power levels up to a maximum available power of +12dBm at 102 GHz and for as much as +20dBm at 8 GHz when biased in the off-state.

PUBLICATIONS:

1. P. Marsh, D. Pavlidis and K. Hong, "InGaAs-Schottky Contacts made by In-situ Plated Evaporated Pt," *EEE Trans. on Electronic Dev.*, **45**, 1-12, 1998.

2. E. Alekseev, D. Cui and D. Pavlidis, "Power-Handling Capability of W-Band InGaAs Pin Diode Switches," *Proceedings of the IEEE International Conference on Indium Phosphide and Related Materials* (IEEE-IPRM 98), Tsukuba, Japan, pp. 199-202, May 11-15, 1998.

3. E. Alekseev, D. Pavlidis and C. Tsironis, "W-band On-Wafer Load-Pull Measurement System and Its Application to HEMT Characterization," *IEEE MTT-S International Microwave Symposium Digest*, Baltimore, MD, **3**: 1479-1482, June 7-9, 1998.

Ph.D. STUDENTS GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

INTERACTIONS WITH OTHER D.O.D. LABORATORIES, INDUSTRIES AND UNIVERSITIES:

TRW	JPL
Technical University of Darmstadt	Raytheon

X. GROWTH OF NOVEL MATERIALS FOR DEVICE APPLICATIONS

FACULTY SUPERVISOR: P. Bhattacharya

RESEARCH SCIENTISTS: K. Kamath
W.-Q. Li
X. Zhang
Y. C. Chen

GRADUATE STUDENT PARTICIPANTS: H. Gebretsadik
J. Phillips
H. C. Sun
M. Sneed
K. C. Syao

PERIOD: July 1, 1992 – June 30, 1998

TASK OBJECTIVES:

To grow new materials and heterostructures and develop novel growth techniques.

WORK PERFORMED AND SIGNIFICANT ACCOMPLISHMENTS:

Growth of high-quality heterostructures for lasers, transistors and photoreceivers; growth on patterned substrates for multi-wavelength lasers; and self-organized growth.

PUBLICATIONS:

1. H. Gebretsadik, K. Kamath, K. Linder, P. Bhattacharya, C. Caneau and R. Bhat, "Growth and Characterization of Defect-Free GaAs/AlAs Distributed Bragg Reflector Mirrors on Patterned InP-Based Heterostructures," *J. Vac. Sci. Technol. B.*, **16**, 1417, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

INTERACTIONS WITH ARMY LABORATORIES

J. Pamulapati and M. Tobin at ARL
M. Dutta and M. Stroscio at ARO

INTERACTIONS WITH OTHER LABORATORIES, INDUSTRIES AND UNIVERSITIES

Interaction with Hughes Research Laboratories, University of Texas and University of Illinois.

XI. INTEGRATED PHOTORECEIVERS AND THEIR APPLICATIONS TO OPTICAL PHASE-LOCKED LOOPS

FACULTY SUPERVISOR: P. Bhattacharya

RESEARCH SCIENTISTS: H. Eisele
X. Zhang
A. Gutierrez-Aitken
W-Q. Li
Y. C. Chen
K. Yang

GRADUATE STUDENT PARTICIPANT: P. Goetz
A. Gutierrez-Aitken
J. C. Cowles
K. Yang
K. C. Syao

PERIOD: July 1, 1992 – June 30, 1998

TASK OBJECTIVES:

Development of high-performance photoreceivers and photoreceiver arrays for WDM communication.

SIGNIFICANT ACCOMPLISHMENTS:

- Development of InP-based PIN-HBT photoreceiver with 20 GHz bandwidth and -17 dBm sensitivity at 20 GHz.
- Development of 16-channel photoreceiver arrays with record performance.
- Analysis and design of monolithic radiation shields for arrays and demonstration of crosstalk<-40 dB.

WORK PERFORMED AND SIGNIFICANT RESULTS:

Development of InP-based PIN-HBT photoreceiver arrays from growth to circuit characterization.

PUBLICATIONS:

1. P. Bhattacharya, K-C. Syao and A. Gutierrez-Aitken, "1.55μm InP-Based Monolithically Integrated Multi-Channel Photoreceiver Arrays," presented at Photonics West International Conference," San Jose, California, January 24-30, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

P. Goetz, "InP-Based Integrated Optical Phase-Locked Loop for Dense Wavelength Division Multiplexing Laser Stabilization, Ph.D., May, 1998.

INTERACTIONS WITH OTHER D.O.D. LABORATORIES, INDUSTRIES AND UNIVERSITIES:

HRL and University of Illinois.

XII. LOW DIMENSIONAL QUANTUM CONFINED STRUCTURES FOR OPTO-ELECTRONIC DEVICE APPLICATIONS

FACULTY SUPERVISOR: P. Bhattacharya

RESEARCH SCIENTISTS: K. Kamath
T. Brock
W.-Q. Li

GRADUATE STUDENT PARTICIPANTS: L. Davis
K. Ko
J. Shuttlewood
P. Goetz
J. Phillips
D. Klotzkin

PERIOD: July 1, 1992 – June 30, 1998

TASK OBJECTIVES:

Self-organized growth of quantum dots for electronic and opto-electronic device applications.

WORK PERFORMED AND SIGNIFICANT ACCOMPLISHMENTS:

- Demonstrated the first room-temperature quantum dot lasers.
- Demonstrated small-signal modulation bandwidth <20 GHz in QD lasers.
- Characterized carrier dynamics in quantum dots.
- Demonstrated the first QD intersubband detectors at 5-17 μm.

PUBLICATIONS:

No new publications since last report, January, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

P. Goetz, "InP-Based Integrated Optical Phase-Locked Loop for Dense Wavelength Division Multiplexing Laser Stabilization," Ph.D., May, 1998.

D. Klotzkin, "Carrier Dynamics in Quantum Well and Quantum Dot Lasers," Ph.D., May, 1998. Now employed at Lasertron, Lowell, MA.

INTERACTIONS WITH ARMY LABORATORIES:

Joint work with ARL (K. Choi and M. Dutta).

PUBLICATIONS:

1. O. Qasaimeh, K, Kamath, P. Bhattacharya and J. Phillips, "Linear and Quadratic Electro-Optic Coefficients of Self-Organized $In_{0.4}Ga_{0.6}As/GaAs$ Quantum Dots," *Appl. Phys. Lett.*, **72**, 1275, 1998.

2. J. Phillips, K. Kamath and P. Bhattacharya, "InAs/GaAs Self-Organized Quantum Dot Far-Infrared Detectors," presented at the 1998 Conference on Lasers and Electro-Optics, San Francisco, CA, May 3-8, 1998..

XIII. THEORY, FABRICATION AND CHARACTERIZATION OF HIGH SPEED QUANTUM WELL LASERS

FACULTY SUPERVISOR: P. Bhattacharya

RESEARCH SCIENTISTS: A. Gutierrez-Aitken
X. Zhang
Y.-C. Chen
E. Espinoso

GRADUATE STUDENT PARTICIPANTS: M. Gerhold
D. Klotzkin
Y. Yuan
D. Nichols
H. Yoon
H. C. Sun

PERIOD: July 1, 1992 – June 30, 1998

TASK OBJECTIVES:

Development of ultra-high speed quantum well lasers.

SIGNIFICANT ACCOMPLISHMENTS:

Conceived and developed the tunnel injection laser.

WORK PERFORMED:

Designed, fabricated and characterized GaAs-based (0.98μm) and InP-based (1.55μm) tunnel-injection lasers as Fabry-Perot and DFB devices. Demonstrated reduced Auger recombination, chirp, and temperature dependence and enhanced modulation bandwidth ($\sim$50 GHz) in these devices.

PUBLICATIONS:

1. M. Gerhold, A. Onischenko, J. Sarma and P. Bhattacharya, "Novel Design of a Hybrid Cavity Surface Emitting Laser," *J. Quantum Elect.*, **34**, 506, 1998.

PH.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

D. Klotzkin, "Carrier Dynamics in Quantum Well and Quantum Dot Lasers," Ph.D., May, 1998. Now employed at Lasertron, Lowell, MA.

INTERACTIONS WITH ARMY LABORATORIES, OTHER D.O.D. LABORATORIES, INDUSTRIES AND UNIVERSITIES:

J. Pamulapati Army Research Laboratory

XIV. NANOFABRICATION FOR QUANTUM EFFECT DEVICES

FACULTY SUPERVISOR: S. W. Pang

GRADUATE STUDENT PARTICIPANTS: E. W. Berg
K. K. Ko

PERIOD : July 1, 1992 - June 30, 1998

TASK OBJECTIVES:

The objective of this work has been to develop controllable, low-damage etching techniques for quantum scale devices in high-density plasma sources. Due to the small scale of nanostructures, minimizing or eliminating process- induced changes to the surface is crucial for achieving the predicted performance gains on the quantum scale. Both electron cyclotron resonance (ECR) and inductively coupled plasma (ICP) sources have been used to achieve the low damage etch processes with high etch rates, anisotropic profiles, smooth surfaces and high selectivities to masking materials. The effects of etch damage on the material have been shown to be dependent on ion energy, ion density, etch chemistry, etch time, stage temperature, pressure, and source-to-sample distance. Etch induced damage characterization has been done for both the electrical and optical properties of III-V materials and it was found that the etch induced damage may not affect the electrical and optical properties similarly. Schottky diodes, transmission line structures, Hall patterns, and conducting wires were used to evaluate the effects of etching on the electrical characteristics while photoluminescence (PL) measurements on etched quantum wells and quantum boxes were used to evaluate the changes in optical characteristics after etching. Transmission electron microscopy (TEM), Auger electron spectroscopy (AES) and photoreflectance measurements were used to evaluate etch induced modifications in the material properties. In-situ diagnostic methods, including optical emission spectroscopy (OES) and mass spectrometry were used to precisely control the etch depth while etching heterojunction layers. Techniques for minimizing the etch induced damage and improving device performance were developed, including damage removal with low energy species and plasma passivation of surface states. The low damage, high etch rate processes that were developed were used to fabricate in-plane gated (IPG) quantum wire transistors, quantum dot lasers, horizontal distributed Bragg reflector (HDBR) mirrors, microcavities, heterojunction bipolar transistors (HBT), and via holes in InP and GaAs.

SIGNIFICANT ACCOMPLISHMENTS TO DATE:

- Effects of etch-induced damage on III-V materials from dry etching in ECR and ICP high density sources were minimized by using low stage power, low source power,

high Cl_2 percentage, high etch temperature, low pressure, and low source-to-sample distance.

- Quantum boxes and wires were etched with the ECR high-density plasma source for improved PL signal and electro-optic coefficient.
- IPG transistors were fabricated and tested with channel dimensions as small as 100 nm, displaying good FET characteristics and low gate leakage current.
- High reflectivity HDBR mirrors were etched in GaAs with linewidths of 59 nm etched to a depth of 1.5 μm, and 122 nm with a depth of 2.0 μm in InP.
- Passivation and removal of etch induced damage were developed using low energy Cl_2 plasma. Complete recovery and removal of damage were achieved.
- Via holes for MMIC applications were etched using the ECR and ICP sources in InP at room temperature with high etch rates (4.0 μm/min) and smooth vertical sidewalls.
- OES was used for endpoint detection while etching HBT emitters with <5 nm overetching and low surface damage.
- Wafer heating during etching in an ECR plasma source was found to depend on source power, stage power, and pressure. It provides fast etch rates for InP with stage at room temperature.
- Using TEM and AES, it was found that defect density increased with stage power and source power but decreased with stage temperature, and the stoichiometry of GaAs is not affected by etching.
- Etch-induced damage in InGaAs was found to have different effects on the electrical and optical properties with cutoff widths of 136 and 33 nm, respectively.
- Electrical properties of GaAs initially degraded but then improved back towards the control with longer etches. For InGaAs, the degradation increased with etch time.
- Time dependence of etch induced damage on optical properties of GaAs did not show the same effects as the electrical, saturating by 10 s and not changing with etch times up to 40 s.

WORK PERFORMED DURING THIS PERIOD:

- Effect of etch damage on the electrical properties of materials

- Schottky barrier height and reverse breakdown voltage of GaAs diodes decreased while the ideality factor increased with increasing ion energy, indicating increased damage effects.
- The contact resistance of n-GaAs and n- and p-InGaAs increased with ion energy.
- Conducting wires, defined by electron beam lithography with dimensions down to 40 nm, had measured cutoff widths that increased with ion energy.

- Effect of etch damage on the optical properties of materials
  - PL measurements performed on multiple quantum well structures were used to relate etch damage and degradations in PL intensity.
  - The damage depth increased with increasing ion energy.
  - Damage depths greater than the predicted ion penetration depth were found, indicating that ion channeling and damage diffusion play a role in the post-etch damage profile.

- Fabrication of IPG quantum wire transistors using dry etching
  - IPG transistors with channel width between 100 and 1000 nm and gate isolation width ranging from 125 to 1000 nm defined using electron beam lithography.
  - Modulation of a quasi 1-D channel with good FET characteristics achieved using capacitive coupling from in-plane gates. Channel can be completely pinched off with gate-source voltage $\geq$ -0.5 V.
  - Both the drain-source current and gate leakage current increased for IPG transistors etched with higher rf power.

- HDBR mirrors for waveguide lasers
  - HDBR mirrors were etched for InP- and GaAs-based waveguide lasers. These mirrors were 122 nm wide and 2 μm tall for InP and 59 nm wide and 1.5 μm tall for GaAs.
  - Increased wafer temperature using heated surface and plasma heating improved InP etch rate (1 μm/min) and selectivity (62:1).
  - Higher Cl_2 concentration improved selectivity and still maintained vertical profile for InP and GaAs mirrors.
  - Low pressure reduced undercut and microloading.
  - Large process latitude in terms of linewidth or air gap variations. Reflectivity $>$ 90 % maintained for 122 nm wide mirrors even when linewidth was off by $\pm$ 70 nm.

- Precise etch stop for HBTs
  - Response time was 0.3 s for endpoint using optical emission spectroscopy.
  - With optical endpoint using Ga optical emission signal at 417.2 nm, emitter etching could be stopped within ± 3.5 nm. Without optical monitoring, etch depth could vary by ± 20 nm.
  - Dry etched surface roughness measured using atomic force microscopy was 2.5 nm, smoother than the wet etched surface (4.4 nm) and resulted in lower contact resistivity on the p^+-GaInAs base layer.
  - Low surface damage, smooth surface, and short etch time were optimized by two-step etch.
- Via holes and nanostructures in InP and GaAs
  - In the ECR plasma source, etch rates of 2.7 μm/min in InP with vertical profile and smooth surface morphology were achieved at room temperature using a Cl_2 plasma for vias hole 30 μm in diameter and 110 μm deep.
  - In the ICP source, etch rates of 4.0 m/min were achieved in InP with vertical profile and smooth surface morphology. Via holes 10 μm in diameter were etched to a depth of 69 μm using a Cl_2 plasma at 0.25 mTorr.
  - Etch selectivities >300 were achieved using an evaporated Ni mask.
  - Sub-mTorr etching of GaAs for reduced microloading effects. Etching at 0.15 mTorr produced etch rates of >300 nm/min with perfectly vertical profiles.
- Low energy damage removal and passivation of etch induced damage
  - After etching, removal of surface layers by low energy Cl species reduced the residual damage.
  - Plasma passivation of etch induced damage with Cl_2, N_2, N_2/H_2 and H_2S without removal of the semiconductors.
  - Cl_2 plasma passivation restored Schottky diodes and transmission lines to the control characteristics with no detectable etching.
  - Elevated stage temperatures necessary for passivation with N_2, N_2/H_2 and H_2S.
- Uniformity and wafer heating during etching with an ECR source
  - Uniformity better than 5% was achieved across 15-cm diameter wafer.
  - Wafer heating during etching was found to increase with source and stage power.

- Etch rate of InP increased as the wafer temperature increased above 150°C due to plasma heating.
- By cooling the stage with liquid N_2 and flowing He on the backside of the wafer, it was possible to control the temperature of the wafer during etching.

- Effect of etch damage on the material properties of semiconductors
  - TEM measurements revealed that the defect density is found to increase with stage and source power, but decrease with stage temperature.
  - Using AES, stoichiometry of the dry etched GaAs is found to be unaffected and no impurity from the etch mask or the plasma can be detected.
  - PR measurements indicate that Fermi-level position of p-GaAs moves towards midgap due to etch induced defects which are related to As-rich oxide.

- Time dependence of the etch induced damage
  - For GaAs Schottky diodes, the greatest degradation occurred in the first 10 s of etching followed by an improvement in the electrical characteristics.
  - For InGaAs, the contact resistance increased continuously indicating that the etch induced damage was increasing with time, in contrast to the GaAs.
  - The greatest variations in etch induced damage as a function of etch time occurred at higher stage temperature, indicating that defect diffusion is most likely involved.
  - Damage to GaAs, as measured by PL signals from multiple quantum well stacks, did not show an etch time dependence.
  - Most of the time dependent, etch induced damage is confined to the top 15 nm for GaAs but for InGaAs, the time dependent damage was present to depths >25 nm.

PUBLICATIONS:

1. E. W. Berg and S. W. Pang, "Comparisons Between Electrical and Optical Characteristics of Etch Induced Damage in InGaAs," submitted to *J. Vac. Sci. Technol. B*, May, 1998.

2. E. W. Berg and S. W. Pang, "High Aspect Ratio Etching of Nanostructures and Via Holes in GaAs and InP using an Inductively Coupled Plasma System," submitted to *J. Electrochem. Soc.*, April, 1998.

Ph.D. STUDENTS WHO GRADUATED DURING THIS PERIOD:

No Ph.D. students graduated since last report, January, 1998.

INTERACTIONS WITH ARMY LABORATORIES:

- Collaboration with Dr. M. W. Cole to apply TEM analysis on etch induced damage to study defect density and distribution. Also worked with Dr. L. Casas on Auger analysis of surface and sidewall after dry etching and surface treatments. This collaboration resulted in 2 journal articles and 1 conference presentation.
- Collaborated with Dr. P. Cooke on epitaxial layers grown by the MBE for Schottky diodes and transmission lines analysis.

INTERACTIONS WITH OTHERS:

- Joint projects with NTT to develop nanofabrication technologies for optoelectronic devices.
- Joint program with Hughes Research Laboratory to develop controllable etch process and endpoint techniques for HBTs and via holes.
- Joint development with Wavemat Inc. on the optimization of etch uniformity and automatic tuning of ECR cavity.
- Collaboration with Plasma Therm Inc. on inductively coupled plasma source.
- Joint project with GM research laboratory on anisotropic etching of thick polymer and Si layers.
- Joint project with Ford Motor Co. and Advanced Photonix to develop high aspect ratio etching of Si channels for liquid delivery and imaging arrays.
- Joint project with TI and TRW to develop fast and vertical etching for III-V based devices.
- Joint program with Draper Laboratory and Rockwell to develop resonate based microsensors.
- Joint projects with Naval Research Laboratory and NIST to analyze surface defects using photoreflectance and study surface passivation.
- Joint project with Advanced Photonix to develop deep Si channels for imaging arrays.

- Joint program with Motorola to simulate and design integrated Schottky diode process with power MOSFET technology for high speed- power applications.
- Collaboration with ThermaWave Inc. on thermal wave measurements of III-V devices after dry etching.
- Joint project with Microelectronics Center at Technical University of Denmark on applying photoluminescence on dry etching induced defects and damage depth.
- Advised Mohamaad Mazed from JPL on dry etching of GaAs/AlGaAs gratings for DFB laser and re-growth.
- Advised Arnold Yanof from Motorola on dry etching of poly-Si on SiO_2 for xray lithography.
- Advised Karen Seaward from HP for polyimide etching in ECR system.
- Advised Douglas Holmes from Telecom Devices Corp. for InP etching of microlenses.
- Joint project with TI to develop poly-Si gate etching for 64 Mb DRAM.
- Collaborative work with Mark Horn at Lincoln Laboratory, Massachusetts Institute of Technology for high-resolution dry etching of resist and semiconductors.

OTHER INFORMATION:

Editor and Book Chapter - K. Wada and S. W. Pang, "Defects in Optoelectronic Materials", Gordon and Breach, to be published in October, 1998.

XV. MICROMACHINED MICROWAVE CIRCUITS

FACULTY SUPERVISOR: L. Katehi

RESEARCH SCIENTIST: J. East

GRADUATE STUDENT PARTICIPANTS: J. Papapolymerou
F. Brauchler

PERIOD: July 1, 1992 - June 30, 1998

TASK OBJECTIVES:

The goal was to design, fabricate and measure micromachined patch antennas on high dielectric constant materials that have a higher radiation efficiency than conventional antennas and to develop micromachined cavity coupled filters.

MAJOR ACCOMPLISHMENTS:

The goal of this project was to investigate micromaching to fabricate microwave and millimeter wave circuits. The first project involved fabrication of monolithic GaAs based frequency multipliers. A new guiding structure the Finite Ground Coplanar or FGC line was developed. This line is ideal for monolithic applications, since it involves only top side processing, can be used on full thickness wafers and doesn't require via holes. It has very low loss and almost no dispersion for low frequencies to 115 GHz. These lines were used to fabricate a variety of passive and active circuits including filters, stubs, detectors and multipliers. The multipliers were designed for very broadband operation. A fabricated W band multiplier had an output bandwidth greater than 10 GHz.

Micromachining was also used to fabricate high efficiency planar antennas. Typical planar patch antennas on high dielectric materials have low efficiency since they radiate into the high dielectric constant substrate. Micromaching was used to remove material from under the patch, reducing the effective dielectric constant an increasing the efficiency. The experimental efficiency of patch antennas on GaAs substrates increased from 56 to 71micromachining. Finally, micromachining was used to fabricate resonant cavities in semiconductor wafers. Slot coupling was used to couple the lines to microstrip input and output feeds. This allows structures with Q's midway between the large values of waveguide based cavity filters and planar microstrip lines. Experimental Q's of 500 to

600 have been measured.

WORK PERFORMED:

The student that was supported under this project has been transferred to another program.

PUBLICATIONS:

J. Papapolymerou, J. East, L. Katehi, M. Kim and I. Mehdi, "Millimeter-Wave GaAs Monolithic Multipliers," presented at The International Microwave Symposium, Baltimore, Maryland, June, 1998.

INTERACTIONS WITH OTHER D.O.D. LABORATORIES, INDUSTRIES AND UNIVERSITIES:

This work was part of a design study with Texas Instruments. Several of the circuits were also sent to NASA/JPL for evaluation.

ABSTRACTS

(Included in this report are abstracts from current reporting period. Abstracts of earlier publications were included in prior reports)

Resonant Tunneling Diodes: Models and Properties

JIAN PING SUN, GEORGE I. HADDAD, LIFE FELLOW, IEEE,
PINAKI MAZUMDER, SENIOR MEMBER, IEEE, AND JOEL N. SCHULMAN

The resonant tunneling diode (RTD) has been widely studied because of its importance in the field of nanoelectronic science and technology and its potential applications in very high speed/functionality devices and circuits. Even though much progress has been made in this regard, additional work is needed to realize the full potential of RTD's. As research on RTD's continues, we will try in this tutorial review to provide the reader with an overall and succinct picture of where we stand in this exciting field of research and to address the following questions: What makes RTD's so attractive? To what extent can RTD's be modeled for design purposes? What are the required and achievable device properties in terms of digital logic applications? To address these issues, we review the device operational principles, various modeling approaches, and major device properties. Comparisons among the various RTD physical models and major features of RTD's, resonant interband tunneling diodes, and Esaki tunnel diodes are presented. The tutorial and analysis provided in this paper may help the reader in becoming familiar with current research efforts, as well as to examine the important aspects in further RTD developments and their circuit applications.

Keywords— *Nanoelectronics, quantum theory, quantum wells, resonant tunneling devices, semiconductor device modeling.*

I. Introduction

Over the past two decades, resonant tunneling diodes (RTD's) have received a great deal of attention following the pioneering work by Esaki and Tsu [1]. Significant accomplishments have been achieved in terms of RTD device physics, modeling, fabrication technology, and circuit design and applications. The RTD has been widely studied, and well over a thousand research papers have been written on various aspects of this seemingly simple device. Yet, whether RTD's will find their way into mainstream electronics in the future remains inconclusive. The research is ongoing and, in some areas, very active. Why has this device, typically consisting of two potential barriers and one quantum well, been so attractive to the electronics research community for such a long period? With all the knowledge about RTD's so far acquired, will RTD's become practical? What are the main issues of current research on RTD's? To get at these questions, we present in this tutorial review an updated and succinct picture that addresses some important aspects of RTD's. For formal treatments and detailed analysis on specific topics of RTD's, the interested reader can find a number of excellent papers, review articles, and books, which will be referred to in the relevant context. This paper will cover the device aspects, while the circuit aspects on RTD circuit design and digital applications will be reviewed in an accompanying paper in this issue [2].

It is well documented that today's advanced information technology is mainly attributed to the electronic representation and processing of information in a low-cost, high-speed, very compact, and highly reliable fashion, and that the quest and accomplishments of continual miniaturization and integration of solid-state electronics have been the key to the success of the computer industry and computer applications. The advanced multimedia infrastructure and services in the future will demand further reduction in chip size. Chip density, represented by memory technology, has been following Moore's law and has roughly doubled every other year over the last three decades. The trend remains strong and definite, at least for the foreseeable future. For example, a 0.15-μm process technology has been implemented in the first 4-Gb dynamic random access memory (DRAM) unveiled in 1997, and the feature size of DRAM transistors is projected to be 0.18 μm (1 Gb) in 2001, 0.13 μm (4 Gb) in 2004, 0.10 μm (16 Gb) in 2007, and 0.07 μm (64 Gb) by 2010 [3]. A natural and realistic question, then, is whether this desired trend will continue indefinitely. While an ultimate limit on the downscaling of conventional transistors and integrated circuits (IC's) will eventually be reached, device physicists and

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J. N. Schulman was with the Center for Collaborative Research, University of Tokyo, Tokyo, Japan. He is now with HRL Laboratories, Malibu, CA 90265 USA.

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J-198-N

Digital Circuit Applications of Resonant Tunneling Devices

PINAKI MAZUMDER, SENIOR MEMBER, IEEE, SHRIRAM KULKARNI, MAYUKH BHATTACHARYA, JIAN PING SUN, AND GEORGE I. HADDAD, LIFE FELLOW, IEEE

Many semiconductor quantum devices utilize a novel tunneling transport mechanism that allows picosecond device switching speeds. The negative differential resistance characteristic of these devices, achieved due to resonant tunneling, is also ideally suited for the design of highly compact, self-latching logic circuits. As a result, quantum device technology is a promising emerging alternative for high-performance very-large-scale-integration design. The bistable nature of the basic logic gates implemented using resonant tunneling devices has been utilized in the development of a gate-level pipelining technique, called nanopipelining, that significantly improves the throughput and speed of pipelined systems. The advent of multiple-peak resonant tunneling diodes provides a viable means for efficient design of multiple-valued circuits with decreased interconnect complexity and reduced device count as compared to multiple-valued circuits in conventional technologies.

This paper details various circuit design accomplishments in the area of binary and multiple-valued logic using resonant tunneling diodes (RTD's) in conjunction with high-performance III–V devices such as heterojunction bipolar transistors (HBT's) and modulation doped field-effect transistors (MODFET's). New bistable logic families using RTD + HBT and RTD + MODFET gates are described that provide a single-gate, self-latching MAJORITY function in addition to basic NAND, NOR, and inverter gates. This forms the basis for design of high-speed nanopipelined 32- and 64-bit adders using only a single 4-bit adder block. A 32-bit nanopipelined correlator, designed using RTD + HBT logic, demonstrates a simulated power-delay product of 32 pJ while achieving a simulated throughput of one 32-bit correlation every 100 ps. Examples of multiple-valued logic circuits using resonant tunneling devices are presented, which achieve significant compaction in terms of device count over comparable binary logic circuits in conventional technologies. These include a four-valued 4 : 1 multiplexer using four RTD's and 21 HBT's, a mask programmable four-valued, single-input gate using four RTD's and 14 HBT's, and a four-step countdown circuit using one RTD and three HBT's.

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Keywords*—*Logic circuits, multivalued logic circuits, negative resistance circuits, resonant tunneling devices.

I. INTRODUCTION

Growing high-performance computing needs of end users are constantly pushing circuit and device technology to improve in terms of speed and power. Over the past few decades, scaling of device dimensions has proved to be an effective ploy in meeting circuit performance requirements and in decreasing power consumption. As device dimensions in integrated circuits (IC's) shrink from the micrometer to submicrometer levels and below, quantum effects become more prominent. When these device dimensions go down to a few nanometers, quantum effects such as resonant tunneling lead to interesting new device characteristics, which can be exploited to create extremely fast and compact circuits [1]. State-of-the-art commercial process technologies such as complementary metal–oxide–semiconductor (CMOS) rely largely on device scaling for performance improvement of integrated circuits. While this trend has been responsible for rapid advancement of very-large-scale-integration (VLSI) technology in the present era, the physical limits of the conventional device transport phenomenon will likely be reached in the early part of the next century, thus necessitating alternative device concepts to continue fueling the growth of the VLSI industry. The resonant tunneling properties of quantum devices seemingly promise a dramatic improvement in circuit performance as a result of picosecond device switching speeds and reduction in device counts per circuit function. While the properties of resonant tunneling diodes (RTD's) were predicted almost 20 years ago [2], recent developments in growth techniques such as molecular-beam epitaxy have made it possible actually to build and use these devices. Also, to achieve the resonant tunneling phenomenon, it is necessary to scale devices only along a single dimension. This nanometric scaling can be achieved by nonlithographic processes in order to form critical dimensions required for the tunneling effect [3]. This implies that resonant tunneling devices can be integrated with conventional transistors.

Transfer matrix method for interface optical-phonon modes in multiple-interface heterostructure systems

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(Received 6 January 1997; accepted for publication 24 June 1997)

Interactions of carriers with interface optical phonons dominate over other carrier–phonon scatterings in narrow quantum-well structures. Herein, a transfer matrix method is used to establish a formalism for determining the dispersion relations, electrostatic potentials, and Fröhlich interaction Hamiltonians of the interface optical phonons for multiple-interface heterostructure systems within the framework of the macroscopic dielectric continuum model. This method facilitates systematic calculations for complex structures where the conventional method is very difficult to implement. Several specific cases are treated to illustrate the advantages of the general formalism. © *1997 American Institute of Physics.* [S0021-8979(97)03019-3]

I. INTRODUCTION

It is well known that confinement effects modify both acoustic and optical-phonon modes as well as their interactions with carriers in semiconductor nanostructures.[1] For narrow polar–semiconductor quantum wells, carrier interactions with interface optical (IF) phonons play a dominate role in carrier energy relaxation processes.[2] Such narrow quantum-well systems have been of extreme importance in recent studies of unipolar semiconductor lasers, which now produce infrared radiation in room-temperature operation.[3] In theoretical treatments of electron-optical-phonon interactions in heterostructures, both macroscopic[4–9] and microscopic[10] approaches have been applied. Detailed microscopic calculations of optical-phonon modes in polar semiconductors indicate that the dielectric continuum model provides an accurate formalism for modeling electron-optical-phonon interactions.[10] However, most of these theoretical analyses have been confined to highly symmetric and/or simple structures such as single or double quantum wells composed of binary semiconductors. Application of even a simple macroscopic model, not to mention the microscopic *ab initio* models, becomes highly complicated due to the coupling between adjacent interfaces when the structure has multiple heterointerfaces or is asymmetric. At the same time, ternary or quaternary materials may be used along with the binary material systems.

In this work, we develop a general transfer matrix formalism to determine the electrostatic potentials and dispersion relations of IF phonons in a multiple-interface heterostructure (MIH) within the frame work of the macroscopic dielectric continuum model. Furthermore, the optical-phonon normalization condition is generalized to derive the Fröhlich interaction Hamiltonian for IF phonons in this multilayered system composed of polar semiconductors. As in the calculation of electronic envelope functions,[11] the transfer matrix treatment for the IF phonons reduces the complex derivation of the potential to a simple matrix multiplication. A number of examples are provided to illustrate the advantages of the general formalism.

II. TRANSFER MATRIX METHOD

The electrostatic potentials and the corresponding dispersion relations for IF phonons in an arbitrary heterostructure may be obtained by applying the transfer matrix technique in a manner similar to the electronic envelope functions. As is well known, the electrostatic potentials of IF phonon modes[4–9] are linear combinations of exponentially growing and exponentially damped spatial functions. Specifically, for a given IF phonon mode in an n-interface heterostructure, as depicted in Fig. 1(a), the electrostatic potential $\Phi_i(\mathbf{r})$ in the region $\mathbf{R}_i=[z_i,z_{i+1}]$ and its two-dimensional Fourier transform $\Phi_i(q,z)$ are defined by

$$\Phi_i(\mathbf{r})=\sum_{\mathbf{q}} e^{-i\mathbf{q}\cdot\boldsymbol{\rho}}\Phi_i(q,z), \tag{1}$$

$$\Phi_i(q,z)=c_{i-}e^{-qz}+c_{i+}e^{+qz}\equiv c_{i-}\phi_{i-}+c_{i+}\phi_{i+}, \tag{2}$$

where $\boldsymbol{\rho}=(x,y)$ and $\mathbf{q}$ denote the position and wave vector in the two-dimensional plane of the interface. The z axis is chosen as the direction of crystal growth. Furthermore, electrostatic boundary conditions of the dielectric continuum model for IF phonons require that the electrostatic potential and the tangential component of the electric field be continuous;[4–7] thus, $\Phi_i(z)$ and $\epsilon_i(\partial/\partial z)\Phi_i(z)$ must be continuous at each interface. It then follows that at $z=z_i$, i.e., at the interface between the regions $\mathbf{R}_i$ and $\mathbf{R}_{i-1}$,

$$\Phi_i(q,z_i)=\Phi_{i-1}(q,z_i), \tag{3}$$

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 0021-8979/97/82(7)/3363/5/$10.00

Intersubband Relaxation in Step Quantum Well Structures

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Abstract

Intersubband relaxation due to electron interactions with the localized phonon modes plays an important role for population inversion in quantum well laser structures designed for intersubband lasers operating at mid-infrared to submillimeter wavelengths. In this work, intersubband relaxation rates between subbands in step quantum well structures are evaluated numerically using Fermi's golden rule, in which the localized phonon modes including the asymmetric interface modes, symmetric interface modes, and confined phonon modes and the electron-phonon interaction Hamiltonians are derived based on the macroscopic dielectric continuum model, whereas the electron wave functions are obtained by solving the Schrödinger equation for the heterostructures under investigation. The sum rule for the relationship between the form factors of the various localized phonon modes and the bulk phonon modes is examined and verified for these structures. The intersubband relaxation rates due to electron scattering by the asymmetric interface phonons, symmetric interface phonons, and confined phonons are calculated and compared with the relaxation rates calculated using the bulk phonon modes and the Fröhlich interaction Hamiltonian for step quantum well structures with subband separations of 36 meV and 50 meV, corresponding to the bulk longitudinal optical phonon energy and interface phonon energy, respectively. Our results show that for preferential electron relaxation in intersubband laser structures, the effects of the localized phonon modes, especially the interface phonon modes, must be included for optimal design of these structures.

Key words: Localized phonons, Relaxation rates, Intersubband laser.

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ELECTRON-INTERFACE PHONON INTERACTION IN MULTIPLE QUANTUM WELL STRUCTURES

J. P. Sun, H. B. Teng, G. I. Haddad and M. Stroscio

Abstract

Intersubband relaxation rates due to electron interactions with the interface phonons are evaluated for multiple quantum well structures designed for step quantum well lasers operating at mid-infrared to submillimeter wavelengths. The interface phonon modes and electron-phonon interaction Hamiltonians for the structures are derived using the transfer matrix method, based on the macroscopic dielectric continuum model, whereas the electron wave functions are obtained by solving the Schrödinger equation. Fermi's Golden rule is employed to calculate the electron relaxation rates between the subbands in these structures. The relaxation rates for two different structures are examined and compared with those calculated using the bulk phonon modes and the Fröhlich interaction Hamiltonian. The sum rule for the relationship between the form factors of the various localized phonon modes and the bulk phonon modes is verified. The results obtained in this work illustrate that the transfer matrix method provides a convenient way for deriving the properties of the interface phonon modes in different structures of current interest, and that for preferential electron relaxation in intersubband laser structures, the effects of the interface phonon modes are significant and should be considered for optimal design of these laser structures.

The effect of growth interruption on the properties of InGaAs/InAlAs quantum well structures

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(Received 1 July 1997; accepted for publication 14 November 1997)

The effect of the growth interruption time during the growth of InGaAs/InAlAs quantum well structures is shown to have a significant effect on both the interband transitions, as determined by photoreflectance, and the electrical properties of the as-grown structure. The results show that, for increasing growth interruption time, the quantum well heterointerfaces become more abrupt and the carrier mobility increases, thereby demonstrating that long interruption times are preferable for the growth of high quality rectangular quantum well structures. © *1998 American Institute of Physics.* [S0003-6951(98)01403-X]

The growth of quantum well (QW) heterostructures is critical as it determines the shape of the QW interfaces and therefore their optical and electronic properties. It is generally assumed that the profile of as-grown QWs is rectangular, although studies[1,2] have found evidence for asymmetry in the QW shape which has resulted in significant changes in the properties of such QW structures.

In this work, the effect of growth interruption times (GITs) on the optical and electrical properties of an InGaAs/InAlAs QW structure is investigated; as differences in GITs are expected to play an important role in determining the shape of the QW profile. Electrical transport properties of these structures as a function of GITs were determined from Hall measurements. Room temperature photoreflectance (PR) was used here to observe the behaviour of QW interband transition energies, which are sensitive to the QW profile, with different GITs. This technique is a powerful post growth characterization tool to analyze the subband structure of QWs.[3,4] A semi-empirical model of subband structure is developed here to identify the transition energies of the InGaAs/InAlAs QW structure.

Three identical InGaAs/InAlAs QW structure with different GITs were grown by MOVPE. Trimethylindium, trimethylgallium, and trimethylaluminum were used for In, Ga, and Al sources, respectively, and 100% arsine and phosphine was used for group V elements. Each structure consisted of a 60 nm $In_{0.507}Al_{0.493}As$ upper barrier layer, a 25 nm $In_{0.53}Ga_{0.47}As$ well layer, and a 300 nm $In_{0.507}Al_{0.493}As$ lower barrier layer grown on an SI InP substrate. All investigated structures reported in this work were undoped. The GITs used here were 0 s, 5 s, and 15 s when switching from barrier growth to well growth and vice versa. All layers were grown at 650 °C, which was found to be the optimum temperature for low background carrier concentration.

A one-dimensional, one-particle, Schrodinger-like wave equation obtained from an envelope function approximation,[5] using a Ben–Denial and Duke model[6] is solved numerically to determine the subband of this structure. The band-gap energy and carrier effective masses are fitted from Ref. 7 and 8 respectively, see Table I. The band offset ratio is taken as 72:28.[9] Other parameters are fitted by Vegard's law linearly using the parameters of binary compounds including AlAs, InAs, and GaAs.

The PR system has been reported previously.[10] The PR spectra of the as-grown QW samples as a function of GITs are shown in Fig. 1. Also shown in Fig. 1 are the calculated transition energies from the model assuming a rectangular QW profile. To simplify the picture only the electron (m) to heavy-hole (n), (H_{mn}), transitions are indicated. The InP substrate and InAlAs barrier signatures at ~1.48 eV and ~1.347 eV, respectively, are readily identified and serve to calibrate the spectra. From Fig. 1, the higher order transitions appear to shift higher in energy with increasing GITs. The

TABLE I. Material parameters used in the modeling calculations. E_g is the band-gap energy, m_e and m_{hh} are the effective masses of electron and heavy hole, respectively.

	Unit	$In_xAl_yGa_{1-x-y}As$
E_g	eV	$0.354x+3.017y+1.432(1-x-y)-0.99xy$ $-0.51x(1-x-y)+0.04y(1-x-y)$
m_e	m_0	$(xy\, m_{e\,InAlAs}+y(1-x-y)m_{e\,AlGaInAs}$ $+x(1-x-y)m_{e\,InGaAs})/(x+y-xy-x^2-y^2)$ $m_{e\,InAlAs}=0.1719-0.1506((1+x-y)/2)$ $m_{e\,AlGaInAs}=0.0632+0.0856(x/2+y)+0.0231(x/2+y)^2$ $m_{e\,InGaAs}=0.0632-0.0419(x+y/2)$
m_{hh}	m_0	$(xy\, m_{hh\,InAlAs}+y(1-x-y)m_{hh\,AlGaInAs}$ $+x(1-x-y)m_{hh\,InGaAs})/(x+y-xy-x^2-y^2)$ $m_{hh\,InAlAs}=0.145-0.121((1+x-y)/2)$ $m_{hh\,AlGaInAs}=0.50+0.2(x/2+y)$ $m_{hh\,InGaAs}=0.5-0.09(x+y/2)$

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11-15 May 1998 Tsukuba, Japan

09:40 - 10:10
ThA1-2 (Invited)

Metalorganic Chemical Vapor Deposition (MOCVD) Material Growth and Application to InP-Based Electronic Devices

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URL: www.eecs.umich.edu/dp-group

Abstract

High Electron Mobility Transistors (HEMTs), Heterojunction Bipolar Transistors (HBTs), PIN, Mixer and Multiplier diodes can benefit tremendously from their design and realization on InP-based material systems. The advantages of InP-based device approaches are multifold and include high mobility and velocity overshoot, as necessary for high-speed operation, heterojunctions appropriate for two-dimensional carrier gases with excellent confinement, bipolar designs with small turn-on voltage and enhanced base and collector transport, and diodes with low-power requirement. The most popular techniques used for realizing the above devices are Molecular Beam Epitaxy (MBE), Chemical Beam Epitaxy (CBE) and Metal Organic Chemical Vapor Deposition (MOCVD). Although MBE has enabled the first demonstration of many of these devices and led to devices with excellent electrical performance, semiconductor device developments using MOCVD showed in most cases comparable electrical performance. Compared to both MBE and CBE, MOCVD also offers a very attractive solution in terms of manufacturing and production needs. Typical features of MOCVD include growth of large batches of wafers, high growth rates, and almost atmospheric growth conditions. This paper reviews the approaches used for MOCVD grown InP-based heterostructures and their application in the demonstration of high-performance electronic devices.

I. HEMT Material Considerations

The three major materials employed in InP-based electronic devices are InP, InGaAs and InAlAs. The impact of growth conditions on crystalline quality, electrical and optical properties of these materials is first studied.

InAlAs can be used as buffer or barrier layer in HEMT structures. High background carrier concentration is usually observed in MOCVD grown InAlAs. This is attributed to deep donors and has been related to oxygen incorporation due to the reactive nature of metalorganic aluminum sources, i.e. TMAl. The creation of deep donor levels is favored at lower growth temperatures, while high growth temperatures appear to result in shallow donors due for example to Si incorporation (1). Growth at 650°C appears to be a good tradeoff and residual levels of mid-$10^{16}cm^{-3}$ have been achieved in this way with good optical characteristics.

Use of InAlAs as buffer can benefit from low temperature growth due to compensation of deep donors by unintentional carbon incorporation. The latter appears to increase as the temperature and/or the V/III ratio decreases (2). Thin (400Å) layers grown at 500°C with a V/III ratio of 70 resulted in 8MΩ/sq resistivity adequate for FETs. Growth at 650°C is, however, necessary for the rest of the HEMT structure.

Of special concern for horizontal transport devices such as HEMTs is the presence of a high carrier concentration at the epi-substrate interface. This has been attributed to various mechanisms, such as iron pile-up and oxygen related deep donors, but the more accepted mechanism is the formation of an atomic silicon spike. This may originate from atmosphere, wafer package, substrate preparation or sources used for growth. Growth of Fe-doped InP buffers does not provide an adequate solution to the elimination of the conductive spike despite the high ($10^8\Omega cm$) Fe-InP resistivities achieved. A high pressure (300Torr) thermal treatment at 670°C in PH_3 reduces buffer leakage, possibly due to Si passivation by Si-O formation (3).

Another alternative for obtaining highly resistive InAlAs buffers is by means of Fe doping which forms a deep acceptor level by virtue of the Fe^{+3}/Fe^{+2} transition. Being a deep acceptor, Fe is more effective than shallow acceptors like carbon in compensating the InAlAs donors. The use of ferro-

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GaInP/GaAs HBT Technology Using TBA, TBP Precursors and Application to Optoelectronic Circuits

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GaInP/GaAs technology is nowadays generally accepted as a good alternative to AlGaAs/GaAs due to the absence of Al and the good etching selectivity of GaInP over GaAs. Since the first demonstration of GaInP HBTs by MOCVD by UofM/Thomson, important progress was made in hydride-free grown materials and devices. This paper reports the development of Chemical-Beam-Epitaxy (CBE) based technology using TBA, TBP, tDMAAs precursors and its application to HBTs and optoelectronic circuits.

The GaInP HBTs had a 7000Å n-GaAs collector ($1.5 \times 10^{16}cm^{-3}$) followed by a 600Å p^+ GaAs base ($4 \times 10^{19}cm^{-3}$) and a tunneling emitter. TBA and TBP were precracked while tDMAAs was injected at room temperature. H_2S and TMGa were used for n and p-doping respectively. The use of tDMAAs allows drastic reduction of sulfur incorporation compared with TBA and thus a very low residual carbon doping ($<10^{15}cm^{-3}$) could be achieved in the collector. Total defect density lower than $10def/cm^2$ was possible with the developed process. Minimum drift of growth parameters was also demonstrated i.e., ~0.27% change of growth rate per month.

The fabricated devices had non-alloyed Ti/Pt/Au for emitter and Pt/Ti/Pt/Au was used for the base. Laterally etched undercut was used for in the base-collector region to reduce the base-collector capacitance while avoiding resistance degradation. HBTs with $2\times30\mu m^2$ emitters had current gain cutoff frequency (f_T) of 60GHz and maximum oscillation frequency (f_{max}) of 100GHz. First reliability tests performed on these devices showed minimum degradation of DC characteristics upon DC bias stress.

Transimpedance amplifiers were designed based on the small- and large-signal characteristics of discrete GaInP HBTs. The basic design had a common-emitter gain stage and the fabricated chips showed a transimpedance gain of 45dBΩ with a bandwidth of 10GHz. A cascode design was also explored for the gain stage and resulted in 47dBΩ gain with 19GHz bandwidth. This design was also found to be less sensitive to large-signal operation due to smaller self-biasing. Eye pattern tests confirmed operation of the transimpedance amplifiers up to at least 10Gbit/sec.

Overall, we present the development of hydride–free CBE technology with highly reproducible growth characteristics and suitability for HBT layer growth. Use of this technology led to good high frequency device performance and reliable characteristics under DC bias stress. Optoelectronic circuits built with such HBTs allowed demonstration of Gbit operation.

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Growth Characteristics of Hydride-Free Chemical Beam Epitaxy and Application to GaInP/GaAs Heterojunction Bipolar Transistors

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We report on the complete characterization of a hydride- and hydrogen-free chemical beam epitaxy (CBE) process for the realization of GaAs/GaInP heterojunction bipolar transistors. Alternative group V sources tertiarybutylarsine, tertiarybutylphosphine, and trisdimethylaminoarsenic are used instead of traditionally employed AsH_3 and PH_3. A very high degree of reproducibility of growth parameters (fluxes, substrate temperature, doping levels) is demonstrated. Total defect densities lower than 10 def/cm^2 are routinely obtained. Large-area GaInP/GaAs heterojunction bipolar transistors (HBTs) show a high current gain of 225 for base sheet resistance of 400 ohm/sq. The devices also exhibit excellent high-frequency characteristics. A cut-off frequency of 48 GHz and a maximum oscillation frequency of 60 GHz have been obtained. These results demonstrate the high potential capability of CBE for high-throughput GaInP/GaAs HBT production.

Key words: Bipolar transistor, chemical beam epitaxy (CBE), GaInP/GaAs

INTRODUCTION

Large development efforts have been devoted to the replacement of highly toxic high-vapor-pressure arsine and phosphine gaseous sources by organometallic compounds in both metalorganic chemical vapor deposition (MOCVD) and chemical beam epitaxy (CBE) technologies. The potential candidates in CBE are trisdimethylaminoarsenic (tDMAAs) and tertiarybutylarsine and phosphine (TBAs, TBP). The last two products have been widely used in the epitaxial growth of GaAs and InP based compounds in MOCVD,[1,2] leading to films of comparable quality to those obtained with arsine and phosphine. The main advantage of these sources is the low vapor pressure compared to arsine and phosphine, resulting in lower concentration and thus minimization of safety risks. From the growth point of view, tDMAAs is a particularly interesting choice since it does not need to be precracked and leads to very low GaAs background doping levels. This is different for TBP and TBAs which have to be precracked. Moreover, although cracking of TBAs is normally almost complete, this is not the case for TBP, which suffers from a relatively low cracking efficiency. CBE material quality has been demonstrated to be compatible with such HBT designs[3,4] as well as laser devices.[5] Since the first demonstration of GaInP/GaAs HBTs by MOCVD,[6] important progress was made in hydride-free grown related materials and device properties. In this paper, we present results on the establishment of a reproducible manufacturing process for realizing carbon-doped GaAs/GaInP HBTs using a complete hydride-free gaseous growth process on $3 \times 2''$ or $1 \times 4''$ wafers.

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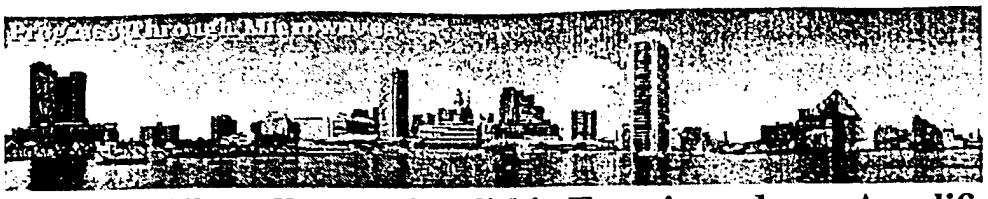
GaInP and GaAs CBE Material Technology

The experiments reported in this work were carried out in an all-gaseous-source $3 \times 2''$ VG90 machine. The gas-source configuration employed is the following: group III atoms are provided by conventional organometallic sources (triethylgallium [TEGa] and trimethylindium [TMIn]); precracked TBP, TBAs, and uncracked tDMAAs are the group V starting sources. Uncracked hydrogen sulfide (H_2S) and trimethylgallium (TMGa) were used for n-type and p-type doping, respectively. All the gas sources are regulated using a two-valve pressure control system. The pressure control system permits a very high level of reliability and flux reproducibility. The latter is a key parameter in a production environment since the cost of an epilayer device structure is strongly influenced by the calibration runs. This aspect represents one of the main advantages of the CBE technology and is illustrated in Fig. 1. This figure shows the evolution of the growth rate of GaAs as a function of time. The measurements represent reflection high



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GaInP/GaAs HBT Broadband Monolithic Transimpedance Amplifiers and Their High Frequency Small and Large signal Characteristics

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Abstract - Monolithic broadband transimpedance amplifiers were developed using GaInP/GaAs single HBTs. The HBTs showed a cut off frequency (f_T) of 60GHz and maximum oscillation frequency (f_{max}) of 100GHz. The fabricated amplifiers had a maximum bandwidth of 19GHz and an associated transimpedance gain of 47dBΩ. The large signal characteristics of two transimpedance amplifier designs with similar gain were also investigated and showed that the cascode approach is much less sensitive to input power level.

1. Introduction

High speed and high capacity transmission systems are necessary for next generation optical communications. Considerations made in the development of such systems include process yield which is related to cost reduction, performance stability and device life time under actual circumstances.

AlGaAs/GaAs HBT preamplifiers based on advanced p+ regrown extrinsic technology have demonstrated excellent performance (34.6GHz) with a transimpedance gain of 41.6dBΩ [1]. GaInP/GaAs Heterojunction Bipolar Transistors (HBTs) are well known alternatives over AlGaAs/GaAs HBTs due to their attractive features such as excellent etching selectivity which contributes to process yield, device reliability [2] and improved carrier injection efficiency [3],[4] due to their large valence band discontinuity. GaInP/GaAs HBT monolithic transimpedance amplifiers can be used for short distance communication (0.8μm) such as board-to-board or chip-to-chip data links but also as an alternative solution to InP-based technology for long distance communication (1.3~1.5μm) by means of flip chip hybrid mounted InP photodiodes.

This paper describes the design, fabrication and high frequency characteristics of transimpedance amplifier OEICs using the GaInP/GaAs HBT approach. Their small but also large signal characteristics are reported since the latter can become an important issue when the front-end preamplifer receives large power signals as often occurs from a photodiode in optical receiver systems [5].

2. HBT Technology and Performance

The GaInP/GaAs HBTs were fabricated on layers which were grown by a specially developed hydride and hydrogen-free Chemical Beam Epitaxy (CBE) process which guaranteed a very high degree of reproducibility of growth parameters with small defect content and high output capability [6]. Self-aligned GaInP/GaAs single HBTs were fabricated on these layers using simple all wet chemical etching which minimized layer damage and device degradation. Ti/Pt/Au non-alloyed metal was deposited to emitter and collector layers while Pt/Ti/Pt/Au was used as the base metal. Laterally Etched undercut (LEU) was developed and applied between the base and collector region to reduce base-collector capacitance (C_{BC}) while avoiding base resistance degradation. More details about the fabrication process have been presented elsewhere [7]. Fabricated devices were measured using a network analyzer from 0.5 to 25.5 GHz. A

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Application of photoreflectance spectroscopy to the study of interface roughness in InGaAs/InAlAs Heterointerfaces

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InGaAs-Schottky Contacts Made by *In Situ* Plated and Evaporated Pt—An Analysis Based on DC and Noise Characteristics

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Abstract— **The choice of plated versus evaporated Pt Schottky anode formation technology is shown to have a significant impact on junction quality and the noise temperature of InGaAs mixer diodes. The investigated diode layers were grown in-house via *M*etalorganic *V*apor *P*hase *E*pitaxy (MOVPE) on an S.I. InP wafer. For anode diameters at and below 2 μm, plated anodes clearly show superior fabrication (~80%) yields relative to evaporated (below ~5%). DC and low-/high-frequency noise characteristics were compared, as functions of dc current drive, for plated versus evaporated InGaAs Schottky contacts at 10 Hz–100 KHz and 1.4 GHz for 4- and 6- μm anode diameters. Plated anodes show distinctly lower ideality factors of ~1.2 versus ~1.4–1.66 for evaporated anodes. Plated Schottky contacts showed 5.5 dB lower noise levels in the range of 10 Hz–100 KHz and a lower noise temperature (220 K versus 360 K) at 1.4 GHz. Overall, relative to conventional evaporated Pt, plated Pt anode technology offers superior fabrication yield and should lead to higher receiver sensitivity especially when low IF frequencies are used.**

I. Introduction

CURRENTLY, the lack of good low-noise amplifiers above ~100 GHz implies that the noise temperature of high-sensitivity receivers operating at such frequencies is limited by the mixer. The expense of LO power at millimeter and submillimeter-wave applications makes it imperative to employ technologies which reduce LO power requirements and/or reduce the LO frequency by using subharmonic mixers. Since the antiparallel-connected diode pairs used in subharmonic mixers are difficult to bias, the low Schottky barrier height (ϕ_b), of InGaAs reduces the required P_{LO} relative to GaAs. Indeed, InGaAs mixer technology [1], [2] has recently demonstrated near state-of-art performance while requiring significantly less LO power (P_{LO}) than GaAs diodes, especially in zero-bias applications [3], [4]. Relative to GaAs, the higher electron mobility of InGaAs should contribute to reduced ohmic contact resistance, consequently reducing mixer noise temperatures especially at high frequencies. InGaAs mixers have also been integrated with other receiver elements [2]–[4], making them very interesting for potential use in integrated InP-based millimeter and submillimeter-wave receivers.

One of the more critical factors determining mixer noise temperature is the quality of the Schottky junction. High-quality Schottky contacts will reduce mixer noise by decreasing the ideality factor (η), reducing noise due to electron trapping in the vicinity of the Schottky contact, and reducing reverse leakage. A plated Pt GaAs Schottky technology was shown to reduce trap densities [5] and low-frequency noise [6] in GaAs Schottky diodes. The formation of some of the traps in [6] was attributed to the damage due to high-energy electrons impinging the GaAs during the deposition of the Schottky contacts via E-beam metal evaporation. The plated Schottky process allegedly eliminates damage due to impinging electrons as well as surface damage because it does not employ E-beam metal evaporation and the GaAs surface is slightly etched before plating which removes any surface damage and oxides. The elimination of surface oxides and surface damage via *in situ* etching [7] can also reduce Fermi level pinning [7] and improve the ideality factor [8] via the reduction of trap states [5] and electron barriers [8], due to surface damage and oxide layers [9].

During the optimization of InGaAs mixers, the authors found that evaporated Ti–InGaAs Schottky contacts had a low ϕ_b combined with very high leakage and ideality factors (η). Techniques for raising the InGaAs Schottky contact ϕ_b and improving η have utilized graded superlattice structures of alternating InGaAs/InAlAs layers [10] or $(NH_4)_2S_x$ chemical surface treatments [11]. The superlattice approach achieved an η of 1.19 with a ϕ_b of 0.71 and 0.60 eV for Au and Cr metals, respectively. However, Au is not recommended as a GaAs Schottky metal due to its high diffusion and low adhesion [12] and it seems likely that this could be the case for InGaAs as well. Based on GaAs results [12] Cr should give reasonable adhesion to InGaAs. However ϕ_b's below ~0.4 eV are desirable for reduction of required P_{LO}, and the author's experience with evaporated Schottky contacts of Ti–InGaAs and Pt–InGaAs appears to indicate that merely adjusting the superlattice of [10] to achieve ϕ_b's below ~0.3–~0.4 eV could potentially result in poor η. Also, the growth of the superlattice increases device complexity and cost and may be difficult

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Indium Phosphide and Related Materials (IPRM'98)

POWER-HANDLING CAPABILITY OF W-BAND INGAAS PIN DIODE SWITCHES

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I. Introduction

One of the most active research areas in the field of radar applications is the development of collision-avoidance systems (CAS) for automotive industry. The first prototypes of HEMT-based CAS chipsets operating at 77GHz have been recently demonstrated [1]. Such chipsets will greatly benefit from the addition of a monolithic transceiver switch, which would allow using a single antenna for both transmission and reception, and thus greatly reduce the cost of the assembly. PIN switching diodes offer unique advantages over HEMTs such as low ON-state resistance and small OFF-state capacitance combined with high power-handling capability [2,3]. Monolithic switches utilizing InGaAs/InP PIN diodes with excellent characteristics have been reported by the authors at W-band frequencies [4]. InP-based switching PINs offer several important advantages over GaAs-based technology, namely: substrate compatibility with high-performance InP-based HEMTs, low DC power consumption, and low ON-state resistance due to high electron mobility and small bandgap of InGaAs. However, the smaller bandgap of InGaAs also manifests itself in earlier onset of self-biasing effects and a smaller breakdown voltage, which affects their power handling. In this work the power-handling capability of InGaAs PIN diodes is reported and compared to that of GaAs PIN diodes. The trade-off between power handling, high frequency performance, and bias conditions is considered. W-band InGaAs PIN diode monolithic switches were fabricated using coplanar-waveguide technology, and their large-signal characteristics measured using a W-band load-pull characterization system are reported for the first time.

II. W-band InGaAs PIN Switches Fabrication

InGaAs PIN layers were grown with our in-house MOCVD system on semi-insulating InP substrates. The investigated structures had the following layers starting from the substrate: 1μm-thick $n^+(1.5\times10^{19}cm^{-3})$, 1μm i(NID $5\times10^{15}cm^{-3}$), and 0.2μm $p^+(1.5\times10^{19}cm^{-3})$. The diodes were fabricated on 5μm-diameter mesas using wet etching with HNO_3:H_2O_2:H_2O (1:1:8) solution. Anodes were made using Pt/Ti/Pt/Au, while Ti/Pt/Au was used for cathode metalization. Identical GaAs-based designs were fabricated for comparison using Pt/Ti/Au and Ge/Au/Ni/Ti/Au correspondingly. All contacts were annealed in Ar at 375°C for 7sec. InGaAs PIN diodes demonstrated turn-on voltage V_{ON}=+0.4V and reverse breakdown V_{BD}=-23.5V (defined at 10μA current), while GaAs PINs showed V_{ON}=+0.9V and V_{BD}=-33V.

W-band monolithic integrated single-pole single-throw switches were fabricated using coplanar-waveguide technology. The switches employed two shunt-connected PIN diodes spaced by λ/4 for improved performance. The layout of the SPST switch is shown in Figure 1. The circuit dimensions were 0.4mm × 1.6mm. Low-parasitic Au-plated airbridge technology was used to connect diodes with the transmission line. Airbridges were also used to connect the two ground planes of coplanar waveguide in order to suppress generation of parasitic wave-propagation modes.

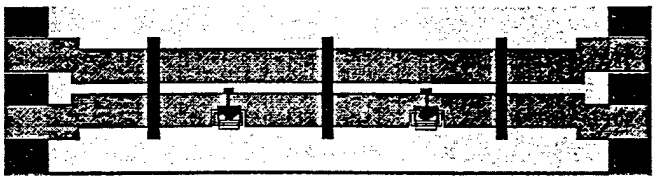

Figure 1. Layout of W-band monolithic integrated InGaAs PIN-diode single-pole single-throw switch

III. Small-Signal Performance

When a negative or zero bias is applied to the anode, the i-layer is depleted of carriers. Only a small charge-displacement current can flow through a small depletion capacitance. The PIN diode is in the high-impedance OFF-state. The signal injected into input port is transmitted to the output port with only a small insertion loss due to the leakage through the diodes.

S-parameters of the fabricated InGaAs PIN diode switches were measured on-wafer at W-band frequencies. The insertion loss (S_{21}) and return loss (S_{11}) of the switch in the OFF-state with bias V_D=-3V are shown in Figure 2.

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W-BAND ON-WAFER LOAD-PULL MEASUREMENT SYSTEM AND ITS APPLICATION TO HEMT CHARACTERIZATION

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ABSTRACT

An on-wafer large-signal characterization system has been developed for W-band frequency applications. The system is computer-controlled and employs a high-precision electromechanical W-band tuner. Its application to obtaining constant output power and gain contours as well as power saturation characteristics of submicron InP-based HEMTs is demonstrated at 77GHz and 102GHz.

INTRODUCTION

Microelectronic devices capable of operation at frequencies of 77GHz and above are necessary for the development of automotive collision-prevention systems and other emerging W-band radar applications [1]. InP-based HEMT is a typical example of device with operation capability at W-band and has been employed for both low noise and high power applications at these frequencies [2,3]. Accurate small-signal as well as large-signal models and good understanding of electrical characteristics is necessary in this frequency range for optimal design of amplifiers and other W-band radar system components. Currently employed techniques are based on either extrapolation of characteristics measured at lower frequencies or on manual testing, which is often limited in range and resolution. The authors have developed an automated W-band on-wafer large-signal characterization system and report for the first time its application to load-pull and power saturation measurements of InP-based HEMTs at 77GHz and 102GHz.

SYSTEM COMPONENTS

The W-band on-wafer large-signal characterization system consisted of a control computer, electro-mechanical W-band tuner, network analyzer, W-band testset, RF and LO sources, frequency multiplier, and two W-band mixers. The RF source was used to generate a 15-22GHz signal, which was then up-converted by a frequency multiplier to produce the 75-110GHz W-band input signal. The source setup also included an isolator for source isolation and protection, an attenuator for input power control, and an EH-tuner for input matching. The maximum output power of this setup was limited to about -2dBm by the frequency multiplier. A 102GHz Gunn-diode oscillator with the output power of 17dBm was also employed to generate a W-band signal at higher power level and drive the tested devices stronger under large-signal conditions.

A 10-dB waveguide directional coupler was used to monitor the input power (P_{in}). Both input and output power were monitored by W-band mixers driven by the LO source, which was phase-locked with the RF source. The benefits from the use of mixers as power meters include frequency selectivity and expanded dynamic range. The schematic of the complete setup is shown in Figure 1.

Load-pull conditions were achieved with the specially developed W-band high-precision computer-controlled FOCUS electromechanical tuner. The control computer measured power, gain, efficiency, and DC-bias as a function of input power and load impedance as set by the load tuner.

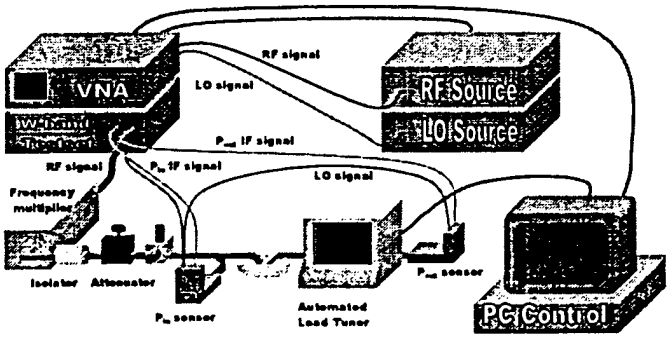

Figure 1. Schematics of an automated W-band on-wafer load-pull measurement system

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Growth and characterization of defect-free GaAs/AlAs distributed Bragg reflector mirrors on patterned InP-based heterostructures

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The growth of defect-free GaAs/AlAs λ/4 distributed Bragg reflector (DBR) mirrors on patterned InP-based heterostructures is demonstrated. The optical quality of the regrown mirror was evaluated using reflectivity and photoluminescence measurements and cross-sectional transmission electron microscopy. It was found that defects did not form or propagate during regrowth of the thick DBR mirror in the mesa structures. In addition, the postregrowth luminescence from the active region remained unchanged. This technique was applied to the fabrication of an InP-based vertical cavity surface-emitting laser designed for 1.55 μm emission. This mirror technology enabled the simultaneous formation of a short-stack Al_xO_y/GaAs DBR mirror and an InAlAs current aperture by the selective wet-oxidation technique. © *1998 American Vacuum Society.*
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I. INTRODUCTION

It has been demonstrated that epitaxial growth of strained layers on patterned mesas or grooves can dramatically reduce the density of misfit dislocations present in the starting substrate[1] or from the strain relaxation process once the critical thickness is reached. The growth thickness can exceed the conventional critical thickness value[2] derived from thermodynamic ground-state considerations.[3] When the mesa size is reduced to the order of a few tens of microns, existing dislocations (possibly originating from the substrate) and surface inhomogeneities are greatly reduced. This inhibits the formation of misfit dislocations by the glide mechanism and the critical thickness is greatly enhanced. The small surface area will also inhibit dislocation multiplication by the Hagen–Strunk mechanism.[4] If, in addition, sources of dislocation nucleation at the mesa edge can be minimized, the epitaxial overlayer on the mesa can be relatively defect free, and linear dislocation densities are less than 100 cm^{-1} along one of the ⟨100⟩ directions.[1] We have previously studied the photoresponse of strained $In_xGa_{1-x}As$ ($0.05 \leqslant x \leqslant 0.20$) $p-i-n$ photodiodes grown in 30–100 μm grooves of 1 μm depth patterned in (001) GaAs substrates.[4] The thicknesses of the diodes were 1 μm, and therefore, much larger than the critical thickness. The diodes exhibited enhanced quantum efficiency and temporal response comparable to similar lattice-matched photodiodes on planar substrates.

Since the lateral dimensions of low-threshold current vertical cavity surface-emitting lasers (VCSELs) vary from 2 to 10 μm and the top distributed Bragg reflector (DBR) λ/4 stack is of similar dimension, it is worthwhile to investigate the possibility of regrowing a GaAs-based DBR directly onto a patterned InP-based VCSEL wafer. Up to now, there have been numerous reports on low threshold (<0.5 mA) GaAs/AlGaAs and InGaAs/GaAs VCSELs emitting at the wavelength range of 0.85–0.98 μm. However, in the wavelength range of 1.3–1.5 μm, suitable for optical fiber communication systems, only a few studies have demonstrated room-temperature, continuous-wave,[5] and pulsed operation[6] of long-wavelength VCSELs. One of the reasons for the slow development of long-wavelength InP-based VCSELs is the difficulty of fabricating high-reflectivity DBR mirrors using lattice-matched layers. The difference in the index of refraction between InP and InGaAsP is only 0.2; therefore, as many as 45 pairs of λ/4 InP and InGaAsP layers are needed to achieve high reflectivity. This presents both epitaxy and processing challenges. The alternate mirror technologies are the dielectric multilayer mirror stack[7] and the wafer-fused GaAs-based mirror.[8] The former inherently gives rise to current injection problems due to its poor electrical and thermal conductivity. The wafer-fusion technology, in which GaAs/AlAs stacks are fused to both sides of the active region of a VCSEL, looks most promising at this time but cannot be applied to full-wafer fabrication yet.

In this paper, the growth of high-quality (defect-free) GaAs-based DBR mirrors on InP-based heterostructures is demonstrated. Both the mirror and the active regions of the VCSEL heterostructure are shown to be of excellent optical quality. We proceed to show that the technique can be applied to make a short-stack high-contrast DBR composed of oxidized AlGaAs and GaAs[9] using the commonly used wet-oxidation technique.[10] In the proposed device, the VCSEL heterostructure would be grown up to the active region and the wafer would be patterned into mesas. The top GaAs-based mirror heterostructure would be grown on it. The VCSEL would then be fabricated by standard photolithography and metallization techniques.

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1.55μm InP-based monolithically integrated multi-channel photoreceiver arrays

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ABSTRACT

We have investigated the performance characteristics of InP-based 1.55μm single and multi-channel photoreceiver arrays consisting of a front-end p-i-n photodiode and a 3-stage HBT-based transimpedance amplifier and realized by single-step epitaxy. The single-channel photoreceiver circuits are characterized by an optical bandwidth of 20 GHz and transimpedance gain of 46 dBΩ. 16-channel arrays, made with the same circuit, demonstrate individual channel bandwidth of 11 GHz. By using a novel monolithically integrated radiation shield, we have been able to reduce the crosstalk to -35 dB at 11 GHz. These parameters represent the best performance in multi-channel integrated photoreceiver arrays. We have performed an electromagnetic full-wave solution of the array, which shows that the measured crosstalk in arrays without the radiation shield could be dominated by radiation crosstalk. The magnitude of the electrical crosstalk in the arrays has also been determined. These results will be presented and discussed.

Keywords: detectors, photoreceivers, arrays

1. INTRODUCTION

High-performance front-end photoreceiver arrays are essential elements of optical-fiber based WDM communication systems. Opto-Electronic Integrated Circuit (OEIC) photoreceivers based on p-i-n photodetectors and Heterostructure Bipolar Transistors (HBTs) have recently demonstrated performance similar to or better than hybrid circuits in terms of sensitivity and bandwidth[1, 2]. The use of a p-i-n diode and HBT as the active devices in the photoreceiver allows a simple scheme of monolithic integration with one-step epitaxy wherein the photodiode is realized using the base, collector and subcollector layers of the HBT structure. This scheme of integration, in which the base-collector junction is used as a photodetector/modulator was first used by us for a GaAs-based integrated controller-modulator logic circuit[3], and later utilized in an integrated photoreceiver by Pedrotti, *et. al.*[4] The important performance characteristics of a photoreceiver array are the operating bandwidth and sensitivity. To improve the sensitivity, noise and crosstalk should be minimized while designing a high performance photoreceiver array. In this paper, the characteristics of single- and multi-channel InP-based 1.55μm photoreceivers are described.

2. EXPERIMENTAL

The design and fabrication of the integrated p-i-n/HBT photoreceivers with self-aligned emitter-base and SiO_x side-wall process have been described elsewhere[5]. The integration scheme and the individual photoreceiver channel with a 3-stage transimpedance amplifier are shown in Fig. 1. The epitaxial heterostructure was grown by molecular beam epitaxy (MBE) on a Fe-doped semi-insulating InP (001) substrate and consists of a standard InAlAs/InGaAs single-HBT. It has a 4000 Å n^+ (1×10^{19} cm^{-3}) InGaAs subcollector, a 6500 Å n^- (5.7×10^{15} cm^{-3}) InGaAs collector that is also used as the absorption region of the p-i-n diode, a 750 Å p^+ (3×10^{19} cm^{-3}) InGaAs base, a 150 Å p-type (2×10^{18} cm^{-3}) InGaAs spacer, a 1500 Å n-type (8×10^{17} cm^{-3}) InAlAs emitter, a 700 Å n^+ (1×10^{19} cm^{-3}) InAlAs layer, and a 1000 Å n^+ (1×10^{19} cm^{-3}) InGaAs contact layer. Ti/Pt/Au metalization was used for the emitter and collector ohmic contacts and Pt/Ti/Pt/Au metalization was used for the base contact. An SiO_x layer is used as an antireflecting (AR) coating for the photodetector and isolation for the interconnection metal. The photoreceiver circuit includes a 156 μm^2 p-i-n photodetector and a three-stage transimpedance amplifier based on 5 μm x 5 μm emitter area

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Linear and quadratic electro-optic coefficients of self-organized $In_{0.4}Ga_{0.6}As/GaAs$ quantum dots

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The electro-optic properties of self-organized $In_{0.4}Ga_{0.6}As/GaAs$ quantum dots have been studied experimentally. Single-mode ridge waveguide structures were grown by molecular beam epitaxy with self-organized $In_{0.4}Ga_{0.6}As/GaAs$ quantum dots in the guiding region. The measured linear and quadratic electro-optic coefficients are 2.58×10^{-11} m/V and 6.25×10^{-17} m^2/V^2, respectively, which are much higher than those obtained for bulk GaAs or quantum well structures. The measured transmission characteristics indicate that low-voltage amplitude modulators can be realized with quantum dot active regions. © *1998 American Institute of Physics.* [S0003-6951(98)01511-3]

Nonlinear optical materials are attractive for their use in optical devices such as switches and electro-optic and electro-absorption modulators. Bulk III–V compounds such as GaAs and GaAlAs exhibit a linear electro-optic (Pockels) effect since they are noncentrosymmetric and lack inversion symmetry. However, the effect is weak compared to that in crystals such as lithium niobate. From the point of photonic integrated circuits, it would be very useful to realize nonlinear electro-optic devices, which could be integrated with other active and quasiactive devices such as lasers, detectors, and interferometers. A great deal of work has therefore been done to investigate the optical properties of quantum wells and superlattices.[1] Quantum wells demonstrate enhanced electro-optic effects due to two features: a built-in birefringence due to the layered structure and a quadratic electro-optic (Kerr) effect arising from the quantum confined Stark effect (QCSE) near the excitonic absorption edge.[2] Low-dimensional quantum confined structures such as quantum wires and dots are expected to exhibit enhanced optical nonlinearities and enhanced electro-optic effects.[3–9]

Various techniques for realizing quantum wires and dots have been reported in the last decade. Quantum structures can be formed by epitaxial growth of quantum wells followed by fine-line lithography, etching, and regrowth—conceptually the most straightforward process—but the results are not very encouraging. In particular, in quantum dots the surface-to-volume ratio can be very large and the resulting nonradiative recombination through surface and interface states can severely degrade the optical properties.[10,11] Other techniques of fabrication have also not been very successful due to dot size nonuniformity or poor interface quality.[12–16] Nonetheless, we did report the measured enhancement of electro-optic effect in small (25–35 nm diameter) $In_xGa_{1-x}As/GaAs$ ($x=0.1$ and $x=0.15$) etched dots.[3] The observed photoluminescence from the dots was very weak and the phase-retardation measurements proved to be difficult. Self-organized growth of strained heterostructures has emerged as a very successful technique for realizing small and defect-free quantum dots with good optical properties.[17–21] Room-temperature lasers with self-organized quantum dots in the active region have been reported recently.[22–24] In this letter, we report the measurement of the electro-optic coefficients of the $In_{0.4}Ga_{0.6}As/GaAs$ self-organized quantum dots from the observed phase retardation in single transverse mode waveguides induced by a transverse electric field. To the best of our knowledge, this is the first report on the electro-optic properties of self-organized quantum dots.

A quantum dot heterostructure was grown by molecular beam epitaxy (MBE), as shown in Fig. 1. The active layer consists of a single layer of self-organized $In_{0.4}Ga_{0.6}As$ quantum dots with a GaAs layer grown over it. The growth conditions are described elsewhere.[23] The grown heterostructure, in fact, forms an edge emitting laser which is suitable for electro-optic measurement. The 30 Å $Al_{0.5}Ga_{0.5}As$ layer is used to tunnel electrons into the quantum dot and to reduce

Contact Layer	p^+ GaAs	0.1μm
Graded Layer	p^- $Al_{1-x}Ga_xAs$	0.2μm
Outer Cladding	p^- $Al_{0.4}Ga_{0.6}As$	1μm
Graded Layer	p^- $Al_{1-x}Ga_xAs$	0.14μm
Inner Cladding	i $Al_{0.15}Ga_{0.85}As$	0.1μm
$In_{0.4}Ga_{0.6}As$ QD's		
Tunneling Barrier	i $Al_{0.5}Ga_{0.5}As$	30Å
Inner Cladding	i GaAs	0.1μm
Graded Layer	n^- $Al_{1-x}Ga_xAs$	0.14μm
Outer Cladding	n^- $Al_{0.4}Ga_{0.6}As$	1μm
Graded Layer	n^- $Al_{1-x}Ga_xAs$	0.2μm
Contact Layer	n^+ GaAs	0.5μm
S.I. (100) GaAs Substrate		

FIG. 1. Schematic of the quantum dot heterostructure grown by molecular beam epitaxy.

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InAs/GaAs Self-Organized Quantum Dot Far-Infrared Detectors

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ABSTRACT

We report far-infrared photoconductivity in self-organized InAs/GaAs quantum dots grown by molecular beam epitaxy. Far-infrared photoconductivity peaked at 17μm is observed from a n-i-n detector structure with doped InAs quantum dots in the intrinsic region.

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Novel Design of a Hybrid-Cavity Surface-Emitting Laser

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Abstract—**A new type of vertical-cavity surface-emitting laser (VCSEL) is proposed and analyzed to show the possibility of optical pumping from an integrated edge-emitting laser. With this scheme, it may be possible to make VCSEL's of very small dimensions and VCSEL arrays. The laser design utilizes dopant induced intermixing of quantum wells (QW's) to provide different gain regions for the surface and edge-emitting sections. The multimode rate equations are used to evaluate the possibility of such a laser and the roles of the various design parameters are discussed. It is seen that efficient surface photon emission is possible for high vertical-cavity mirror reflectivities and sufficient separation of bandgap energies for the two QW gain regions.**

Index Terms— **Optical pumping, rate equations, surface-emitting laser.**

I. Introduction

LOW-THRESHOLD vertical-cavity surface-emitting lasers (VCSEL's) will be important as single devices or as arrays for low-power transmission of optical signals [1]. In larger devices, where threshold current and bandwidth are of minor concern, injection current flow into the active gain region usually takes place through the doped top and bottom mirrors, which are usually in the form of quarter-wave Bragg reflectors [2]. However, as device size is reduced to reduce the threshold current, confining the current through the multilayered mirrors becomes a problem. Considerable success has been achieved with the incorporation of current-constricting apertures in the VCSEL design. These apertures are usually defined by the native oxide Al_xO_y formed by selective wet oxidation of AlAs [3]. Even with this device design, the threshold current increases for device diameters less than 2–3 μm [4]. It is not established yet if this is due to nonradiative recombination at the oxide–semiconductor interface, since the interface state densities have not been measured. Small VCSEL's can of course be photopumped but this does not blend with the practical scheme of things.

The present paper is a theoretical investigation of a novel injection scheme in which the VCSEL is pumped by an integrated edge-emitting device. In such a hybrid-cavity surface emitting laser (HCSEL), shown schematically in Fig. 1, normal current injection of the edge-emitting device produces the edge-emitting or in-plane mode (IPM). A fraction of this mode is absorbed in the gain region of the VCSEL to produce the vertical-cavity mode (VCM), which is emitted. The scheme is analogous to photopumping but is achieved with an integrated and electrically pumped edge-emitting laser. Reflective coatings placed on the facets of the edge-emitting laser will be sown to improve the device performance. This scheme may provide the added advantage of simultaneously exciting an array of small VCSEL's with a single integrated edge-emitting laser.

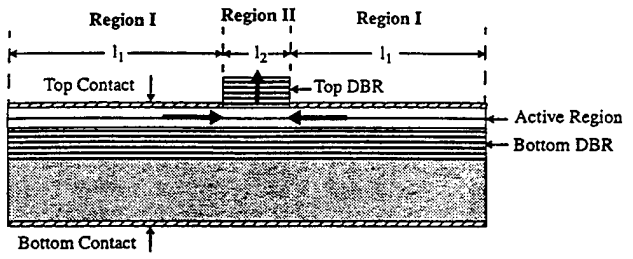

Fig. 1. Schematic of HCSEL.

II. Pumping Scheme with Integrated Edge-Emitting Laser

HCSEL operation is characterized by both in-plane and vertical-cavity modes. The relative proportions depend on the size and configuration of the device. The two modes have been simultaneously used for gain clamping in optical amplifiers [5], photon recycling in edge-emitting lasers [6], and for optical routing switches (which operate in a different regime, i.e., both the VCSEL and edge-emitting laser operate at the same wavelength) [7]–[8]. In the HCSEL, lasing occurs in both modes. With reference to Fig. 1, region I behaves as as an edge-emitting electrically injected laser and region II as a VCSEL that is pumped optically. If the gain region of the HCSEL were uniform, optical pumping would rely on the difference in injected carrier densities in the two regions, i.e., $N_1 > N_2$. This difference is a result of minimal lateral diffusion of injected carriers into region II. The gain curves in Fig. 2 illustrate such a pumping scheme. In this figure, λ_{VC} and λ_{EE} represent the vertical and edge-emitting laser wavelengths (assumed to be at the peak of the gain curves). The edge-emitting laser experiences a gain g_1 in region I and a gain $g_2 < 0$ in region II. The absorbed photons are emitted in the VCM at a gain g_v. In order for this scheme to

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Electrical and Optical Characteristics of Etch Induced Damage in InGaAs

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Abstract

The effects of etch induced damage on the electrical and optical properties of AlGaAs/InGaAs quantum wells (QW) were studied. From the variations in the photoluminescence (PL) intensity and conductivity of etched gratings, the optical cutoff width was found to be 33 nm while the electrical cutoff width was 136 nm. The PL intensity of the gratings indicated that increased stage power during etching causes more damage. Comparisons were also made between the sheet resistivity (ρ_s) of transmission lines and conductivity of wires after etching of AlGaAs/InGaAs and AlInAs/InGaAs QW grown on GaAs and InP substrates, respectively. The AlGaAs/InGaAs QW transmission lines showed reduced ρ_s after etching with higher stage power, although the ρ_s was still higher than the unetched control sample. The AlInAs/InGaAs QW transmission lines had a higher ρ_s as the stage power was increased. The two material systems also showed different etch time and sidewall damage characteristics. The AlInAs/InGaAs QW structure degraded more severely at shorter etch time and had a larger cutoff width as extracted from etched conducting wires.

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Low Pressure Etching of Nanostructures and Via Holes Using an Inductively Coupled Plasma System

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Abstract

A high density inductively coupled plasma (ICP) source has been used for the fabrication of nanostructures in GaAs and via holes in InP. High etch rates, smooth vertical sidewalls, and high selectivity to a Ni mask have been demonstrated with a pure Cl_2 plasma at very low pressure, down to 0.10 mTorr. At a pressure of 0.12 mTorr, a GaAs etch rate of 582 nm/min and a selectivity of 146 to a Ti/Ni mask were obtained. Higher stage powers or lower pressures induced more damage in GaAs. Horizontal distributed Bragg reflector structures were fabricated in GaAs with mirror widths of 150 nm, spaces of 700 nm, and a depth of 2.3 μm. Etching at a pressure of 0.12 mTorr resulted in a higher normalized etch rate compared to etching at 1.30 mTorr in trench widths ranging from 95 nm to 2 μm. Via holes were etched in InP to depths >360 μm. Vertical sidewalls and high etch rates (4.0 μm/min) were achieved with selectivity of 302 to a Ti/Ni mask at a pressure of 0.5 mTorr. The effect of the aspect ratio dependent etching was investigated. It was found that the aspect ratio of the via hole, and not the hole diameter, is mostly responsible for the reduced etch rate in deep trenches.